


GA-MA785GM-US2H

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[illegible]

			
Title			
COVER SHEET			
Size	Document Number		Rev
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Model Name:GA-MA785GM-US2H

Component value change history

Version: 1.3

P-Code: U97028-0

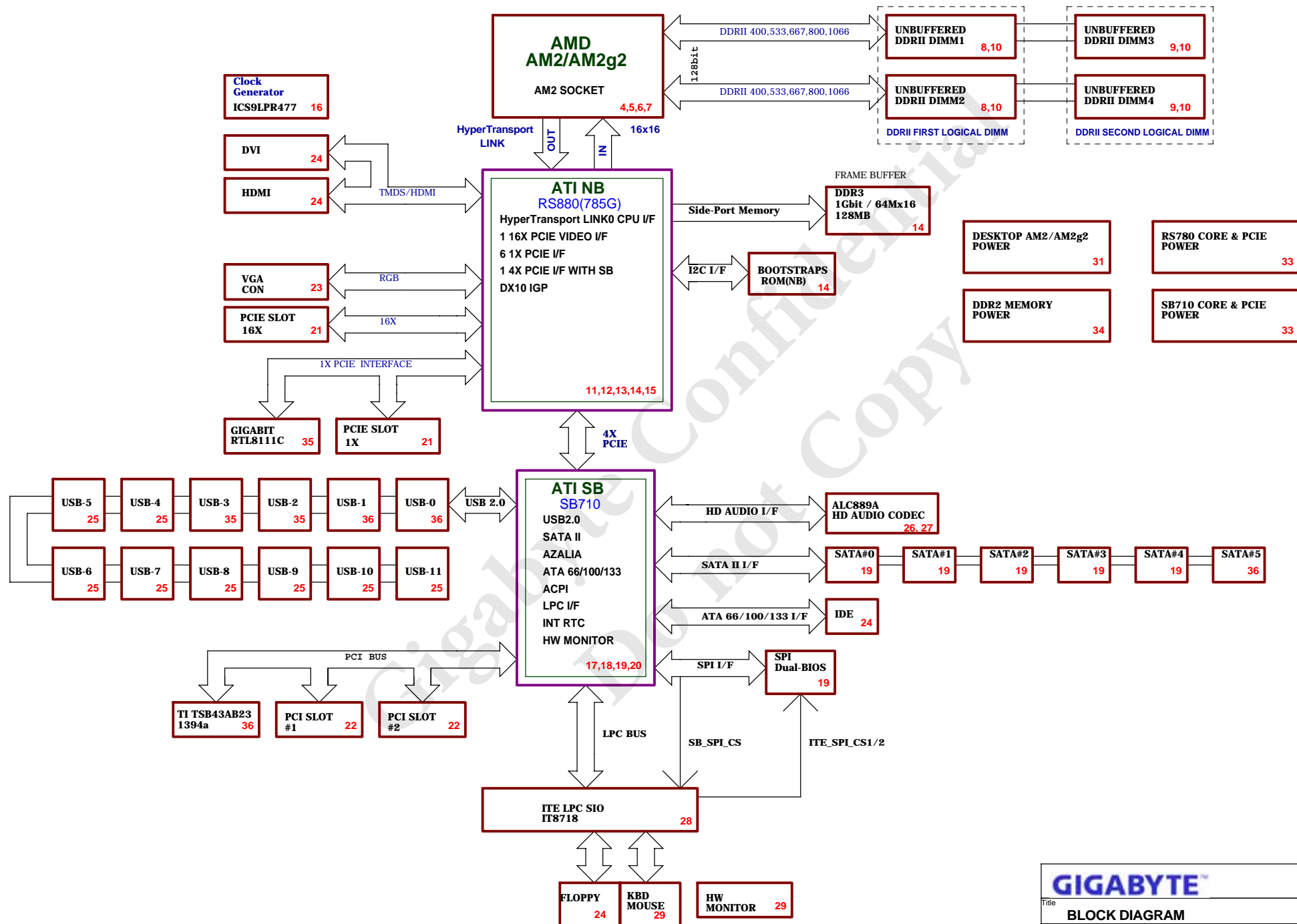
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Circuit or PCB layout change for next version

[illegible]

Title			
BOM & PCB HISTORY			
Size	Document Number	Rev	
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RS880 CUSTOMER DESKTOP REFERENCE DESIGN

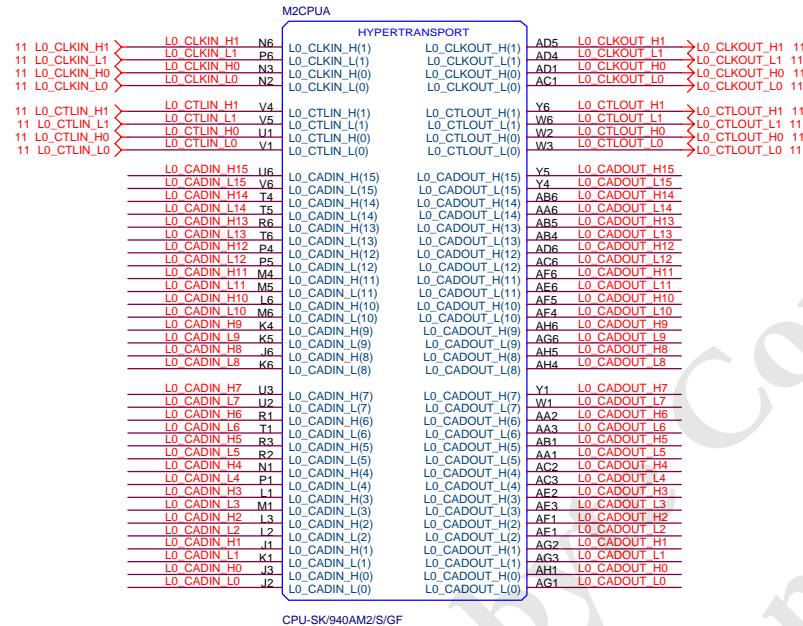


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L0_CADIN_H[0..15] < L0_CADIN_H[0..15] 11

L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] 11
L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] 11

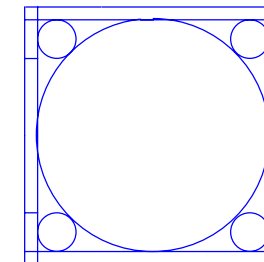
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B



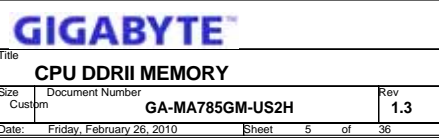
M2CPU

AM3RM/SC/BL/MB[12KRC-04K812-11R]

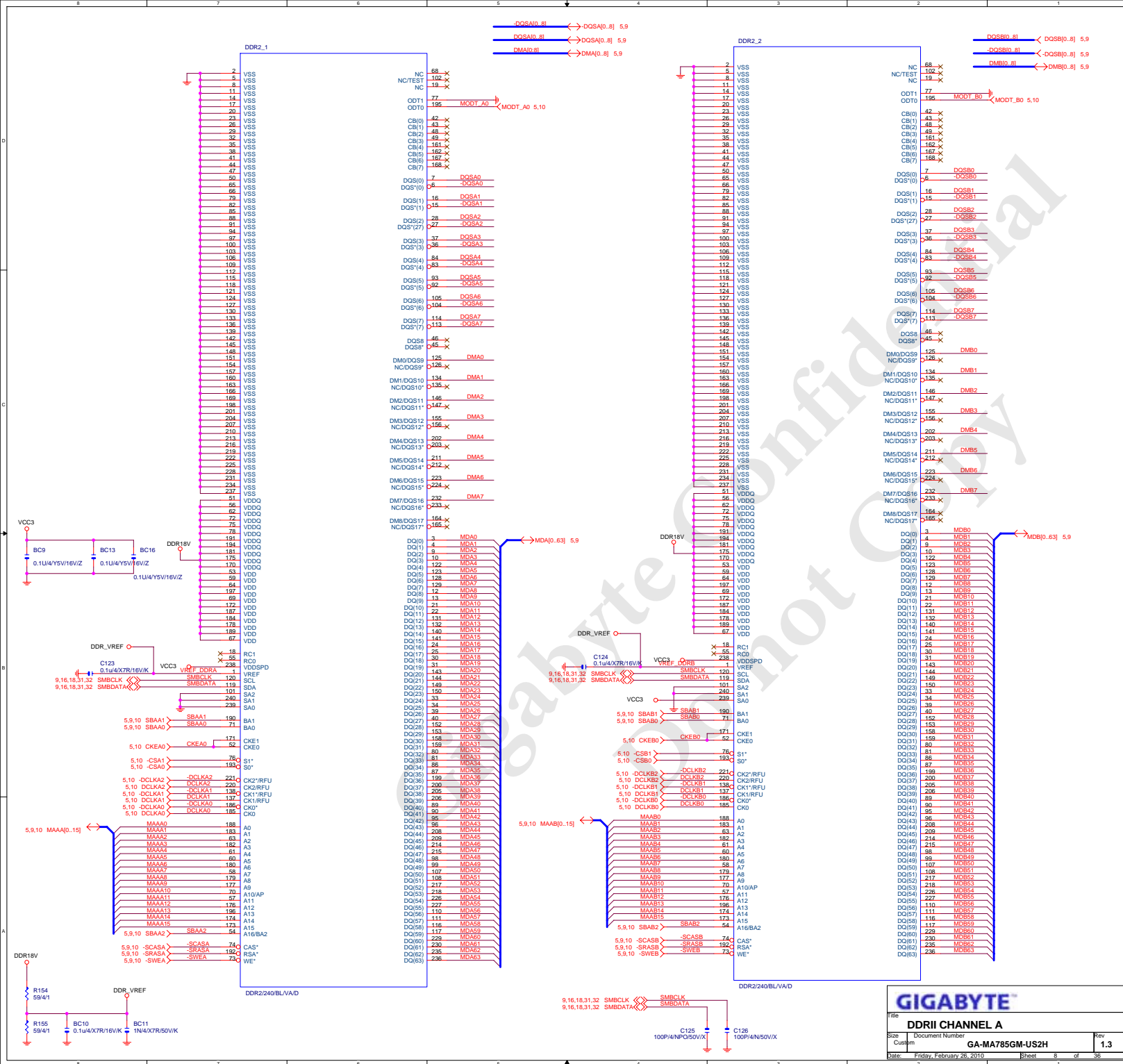


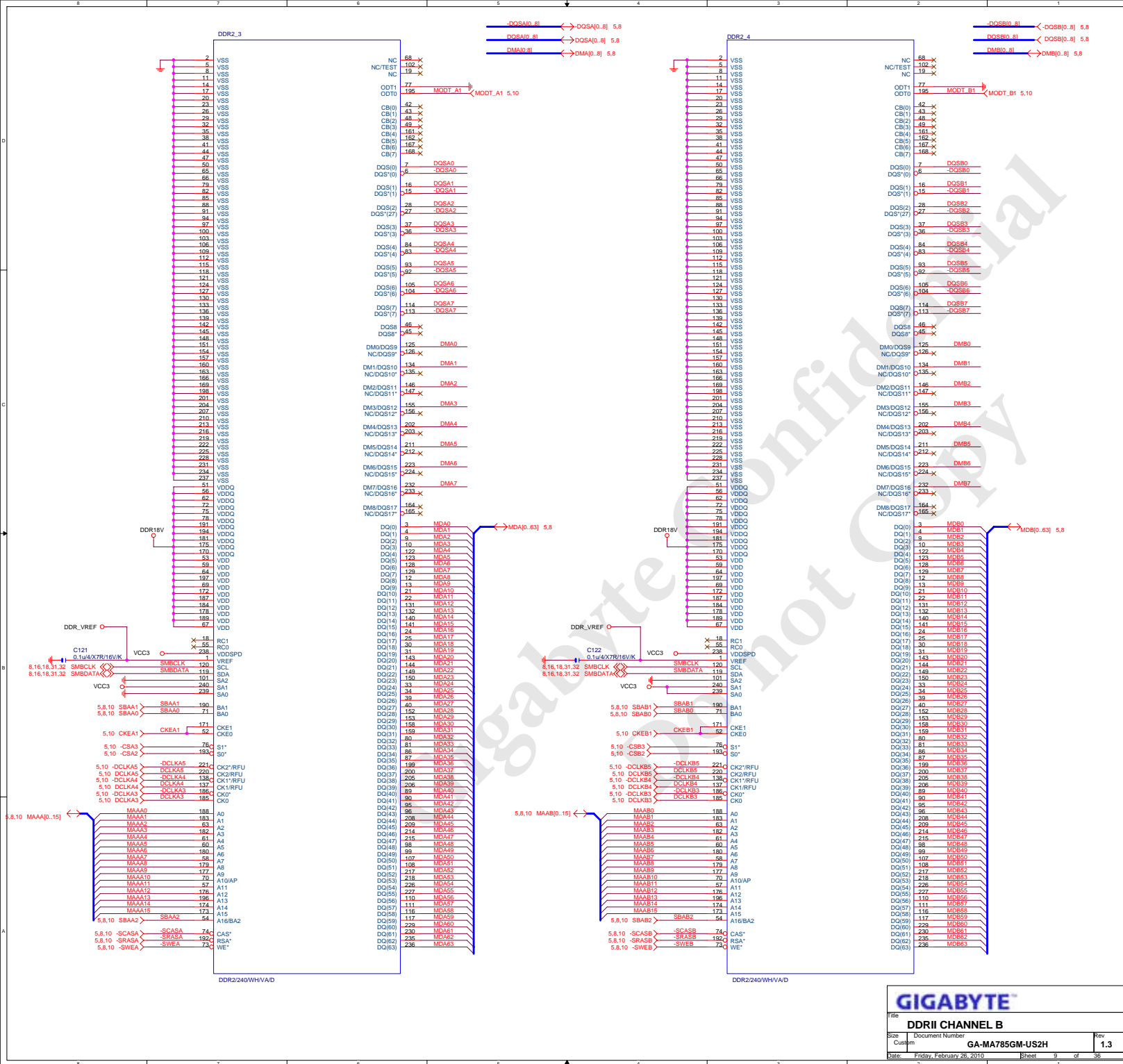
GIGABYTE

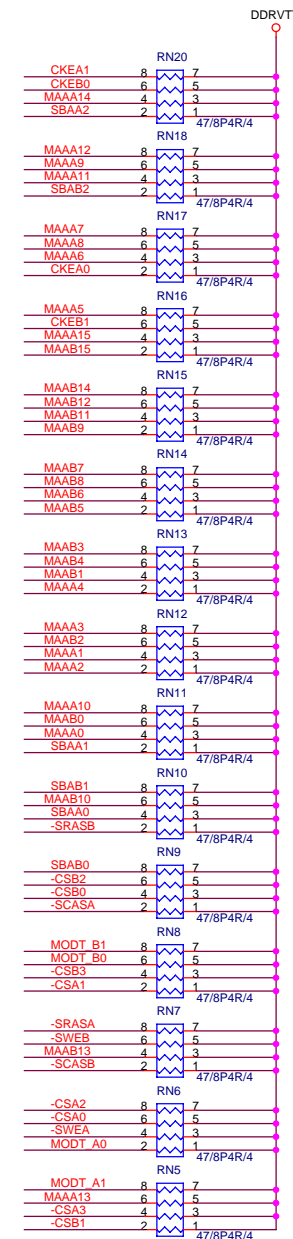
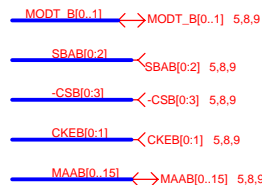
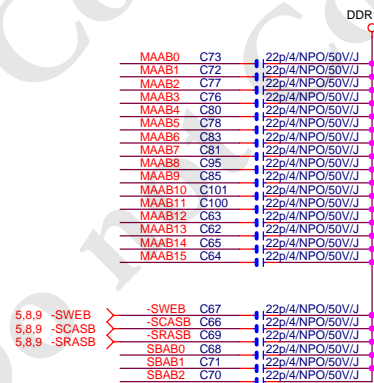
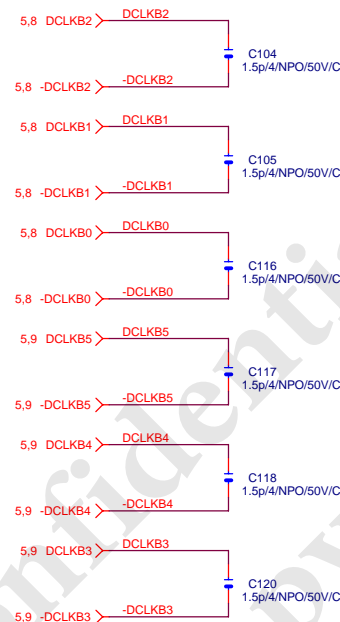
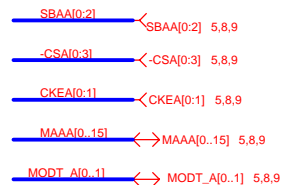
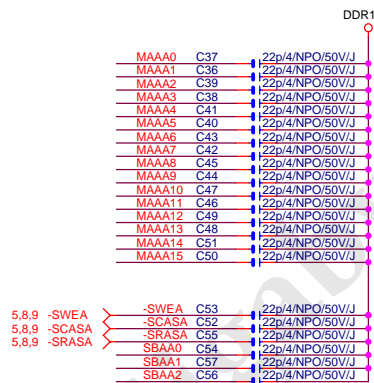
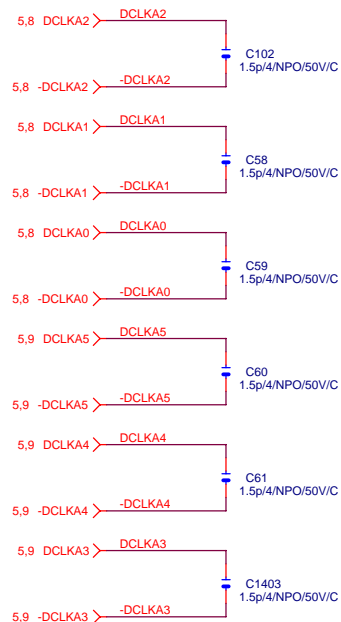
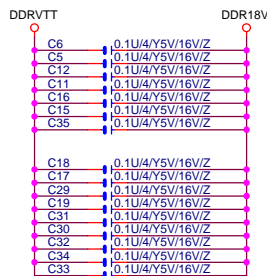
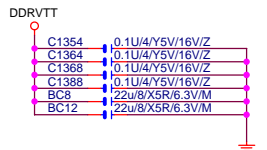
Title CPU HYPER TRANSPORT			
Size Custom	Document Number GA-MA785GM-US2H	Rev 1.3	
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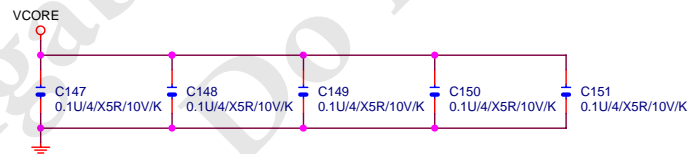
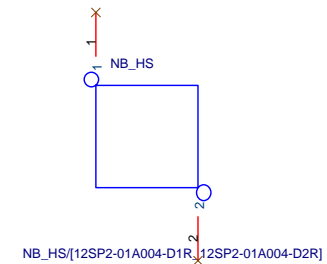






L0 CADIN L[0..15] L0_CADIN_L[0..15] 4
 L0 CADIN H[0..15] L0_CADIN_H[0..15] 4

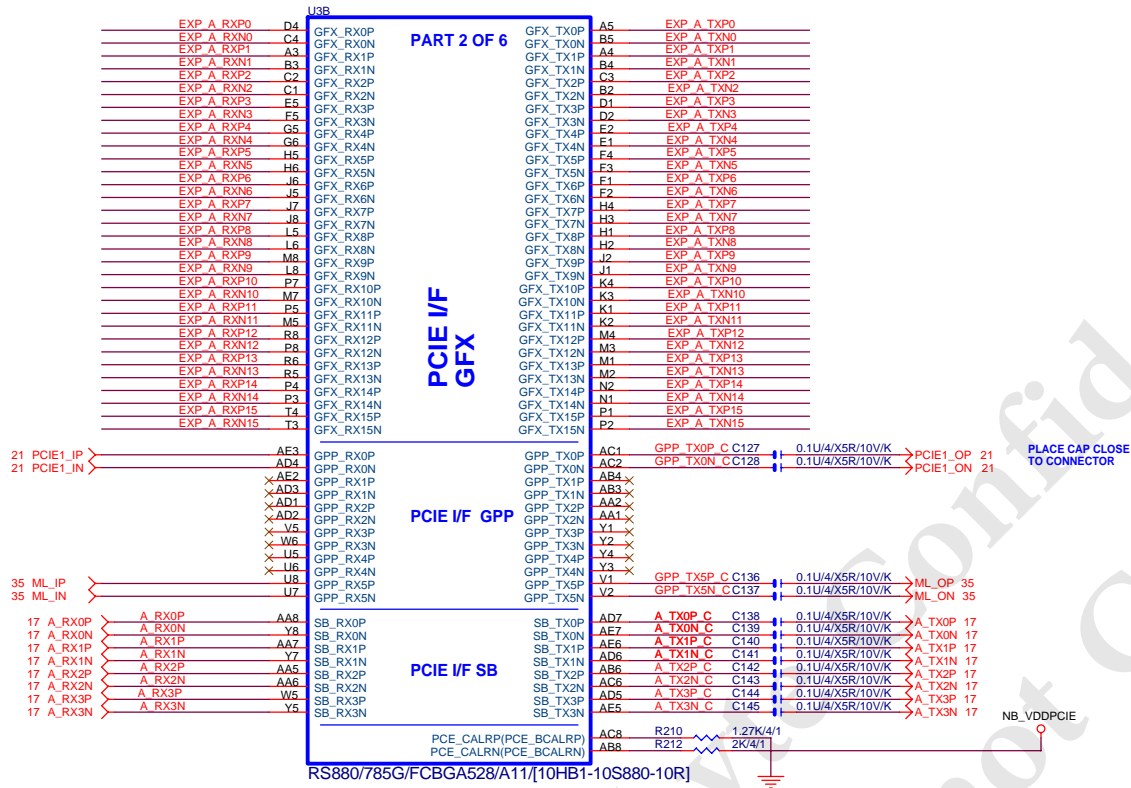
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 L0 CADOUT H[0..15] L0_CADOUT_H[0..15] 4

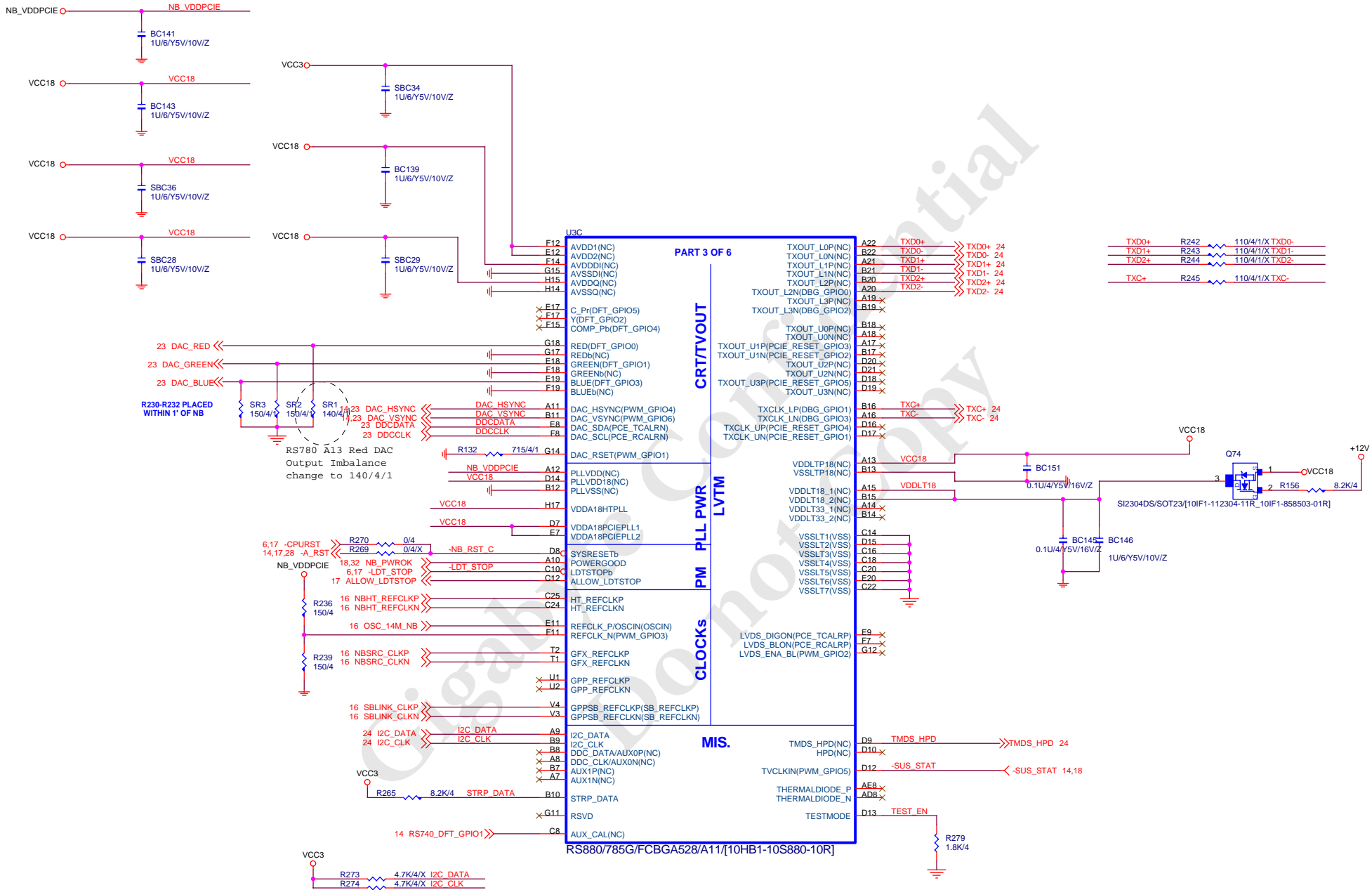


HT Link Stitching Caps

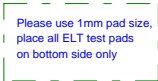
GIGABYTE™		
Title RS880 HT-LINK I/F		
Size B	Document Number GA-MA785GM-US2H	Rev 1.3
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EXP A_RXP[0..15] >> EXP_A_RXP[0..15] 21 EXP A_TXP[0..15] >> EXP_A_TXP[0..15] 21
EXP A_RXN[0..15] >> EXP_A_RXN[0..15] 21 EXP A_TXN[0..15] >> EXP_A_TXN[0..15] 21

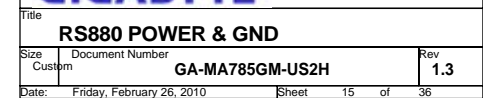




Title			
RS880 SYSTEM I/F			
Size	Document Number	Rev	
Custom	GA-MA785GM-US2H	1.3	
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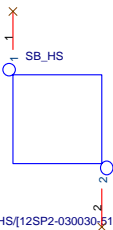
RS880/785G/FCBGA528/A11/[10HB1-10S880-10R]



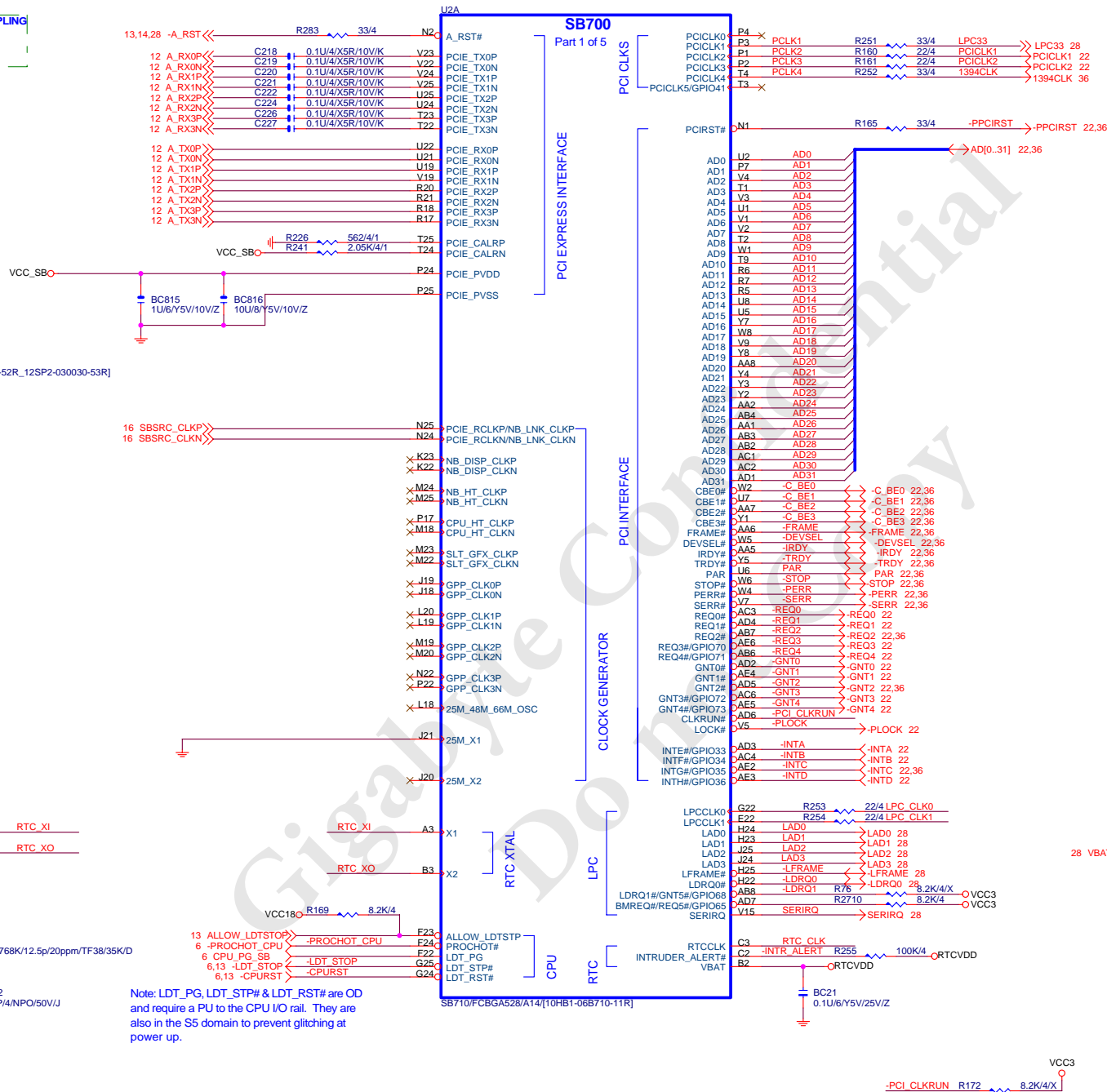


PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO U600

S.B HEATSINK



SB_HS[12SP2-030030-52R_12SP2-030030-53R]



Note: LDT_PG, LDT_STP# & LDT_RST# are OD
and require a PU to the CPU I/O rail. They are
also in the S5 domain to prevent glitching at
power up.

PULL HIGH
WATCHDOG TIMER
ON NB_PWRGD
ENABLED

PULL LOW
WATCHDOG TIMER
ON NB_PWRGD
DISABLED
DEFAULT

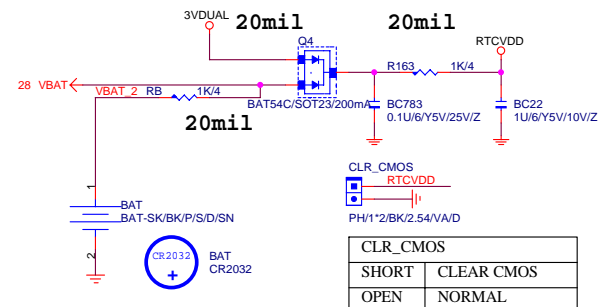
PCLK2
USE
DEBUG
STRAPS

PCLK3
IGNORE
DEBUG
STRAPS
DEFAULT

LPC_CLK0
Rev.A12
IMC
ENABLED
AOD Extreme
DEFAULT

LPC_CLK1
CLKGEN
ENABLED
CLKGEN
DISABLED
DEFAULT

**BIOS after boot setting
EC AOD-ACC**

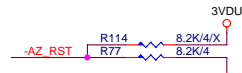
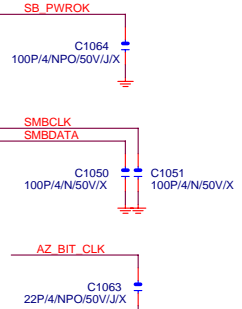
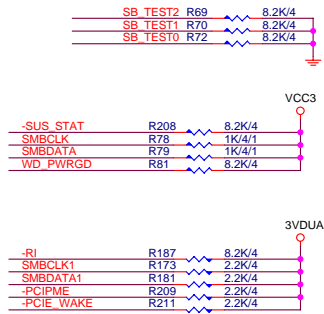


CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

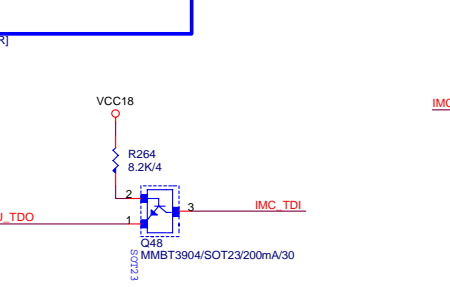
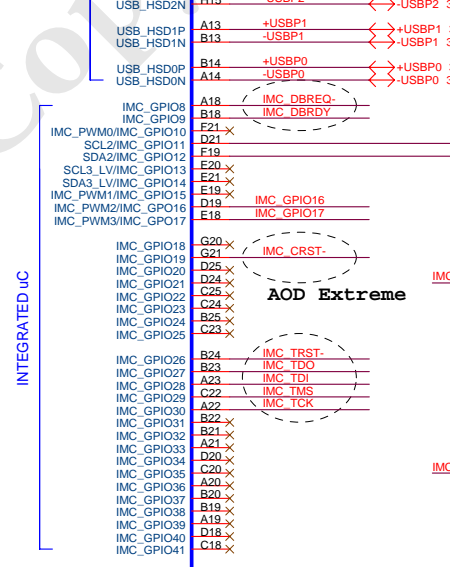
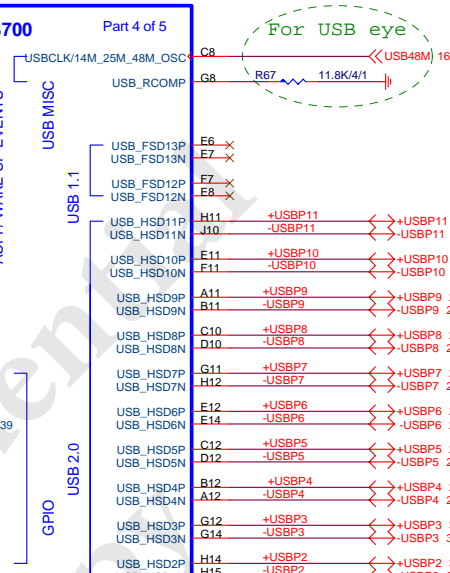
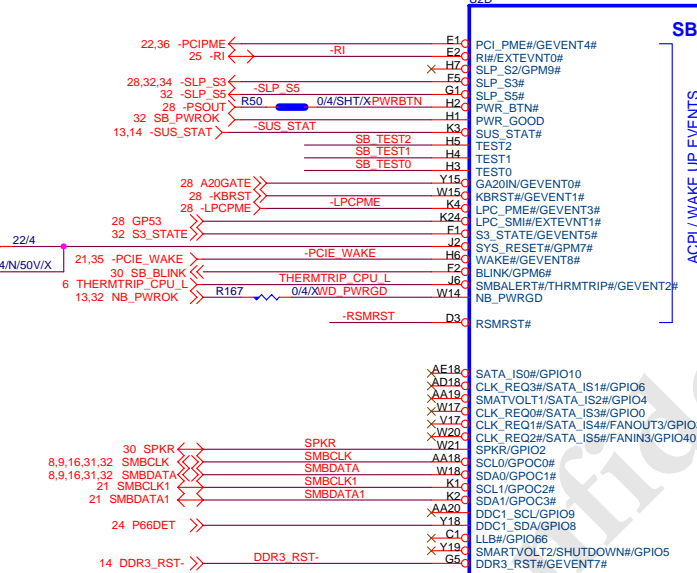
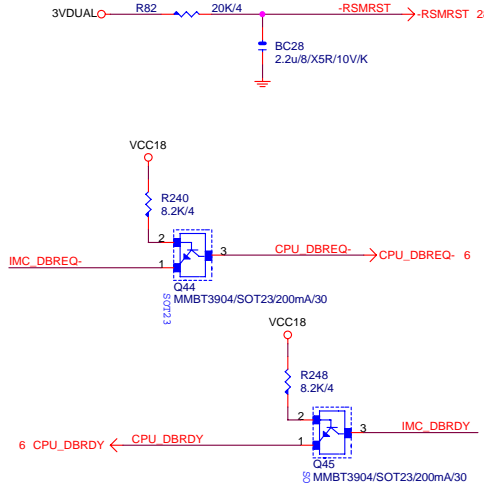
NOT ADD ICT FOR RTCVDD PIN

GIGABYTE

Title ATI SB710 PCIE/PCI/CPU/LPC		
Size Custom	Document Number GA-MA785GM-US2H	Rev 1.3
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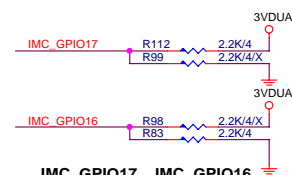


AZ_RST#
Rev. A12
PULL HIGH
PULL LOW

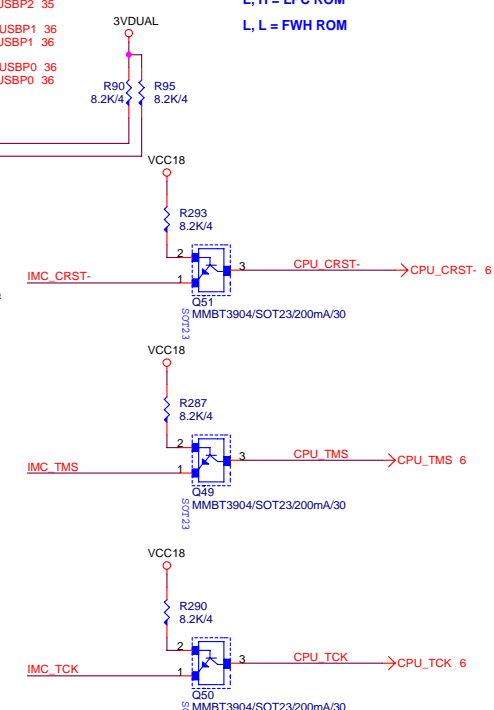


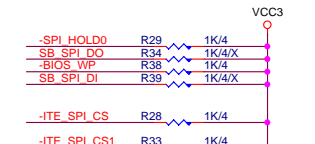
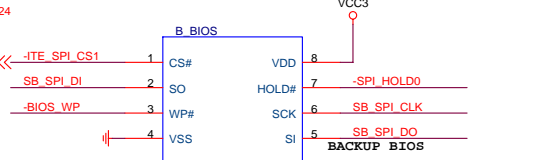
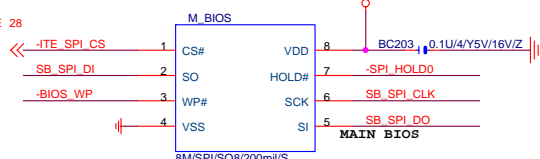
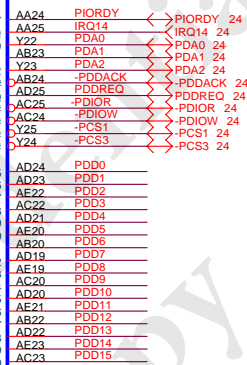
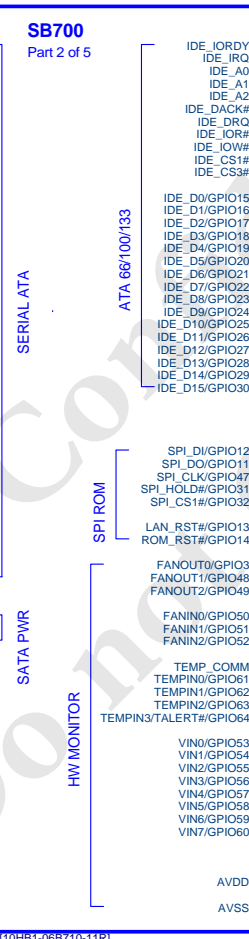
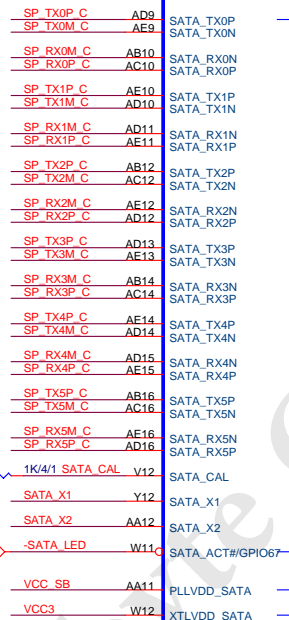
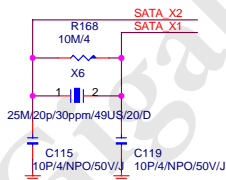
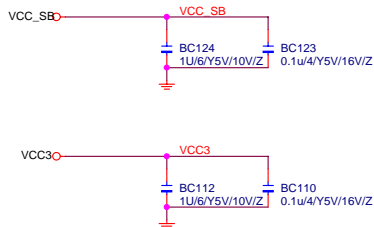
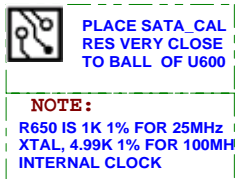
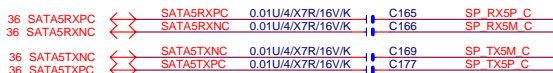
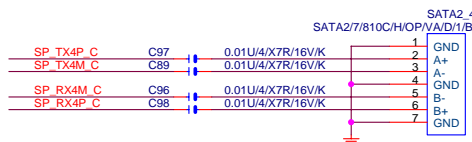
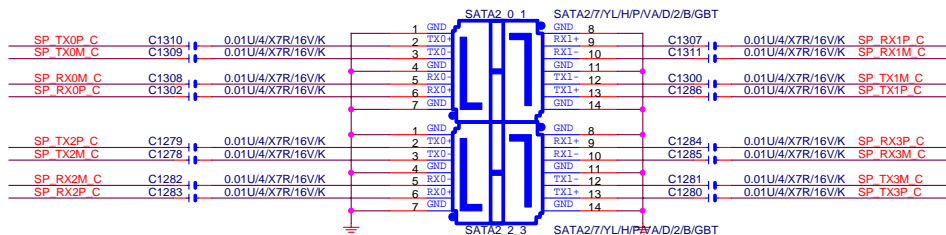
- USB11 FRONT PANEL
- USB10 FRONT PANEL
- USB9 FRONT PANEL
- USB8 FRONT PANEL
- USB7 FRONT PANEL
- USB6 FRONT PANEL
- USB5 FRONT PANEL
- USB4 FRONT PANEL
- USB3 REAR PANEL
- USB2 REAR PANEL
- USB1 REAR PANEL
- USB0 REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer



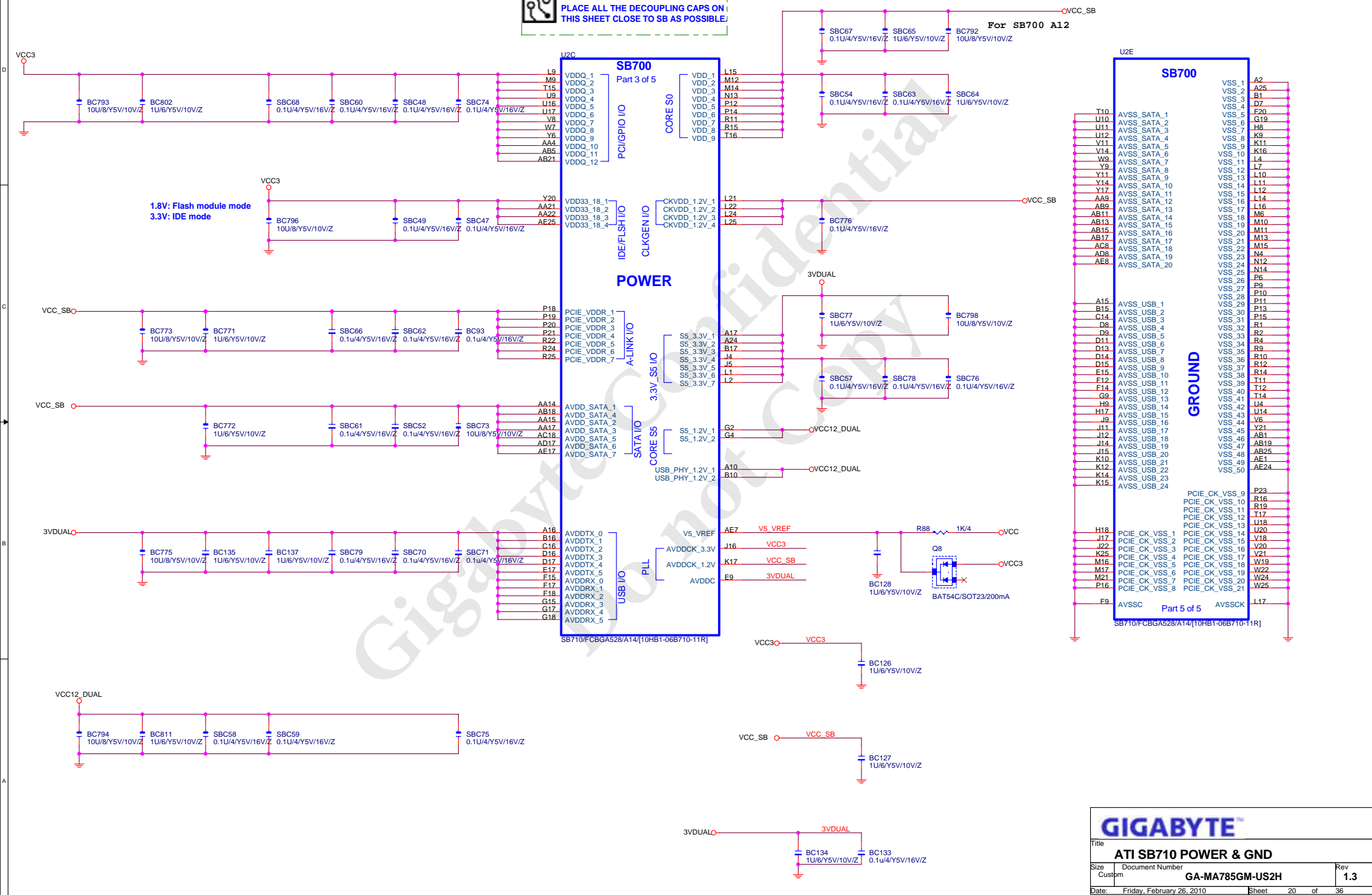
IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FW ROM

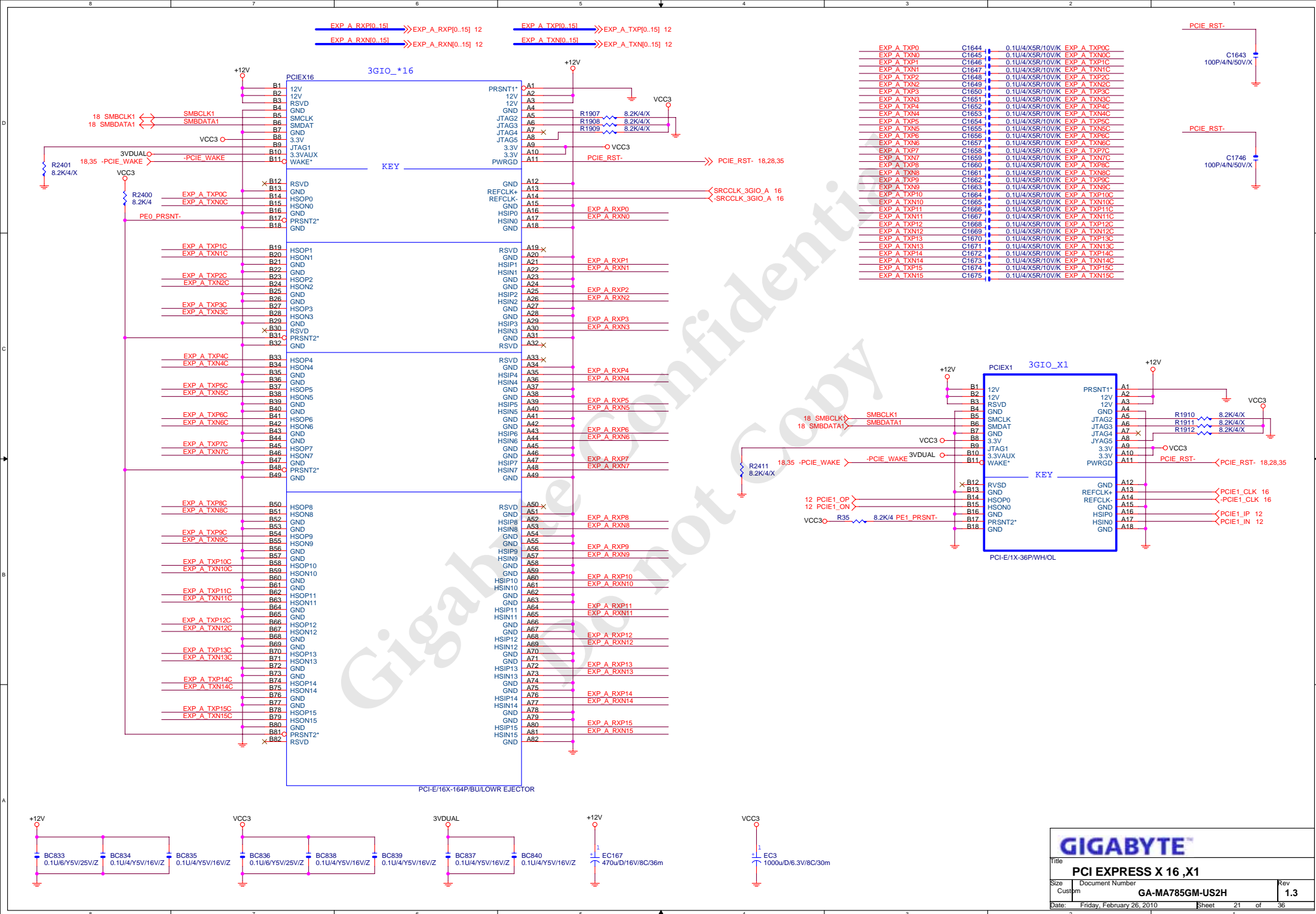






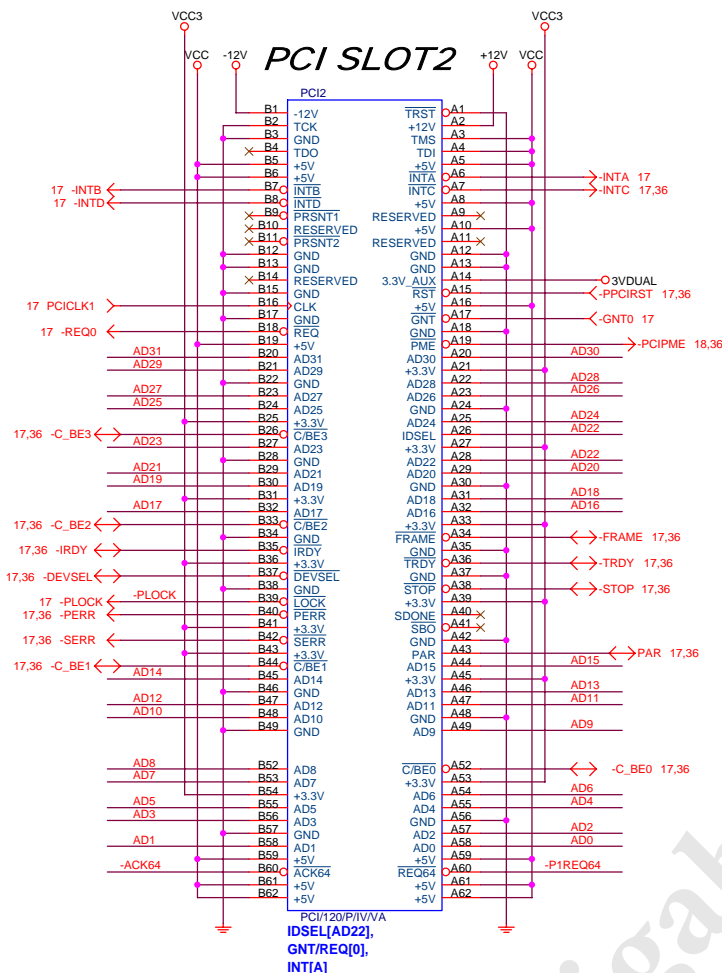
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE



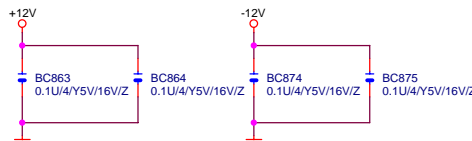
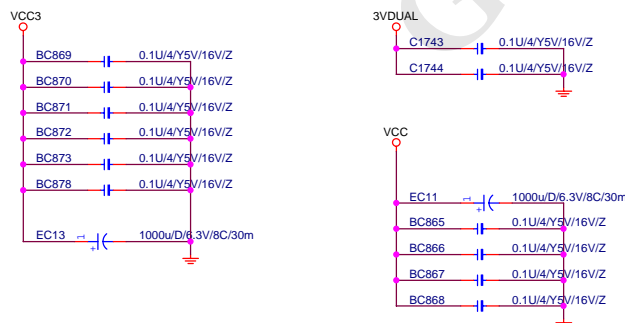
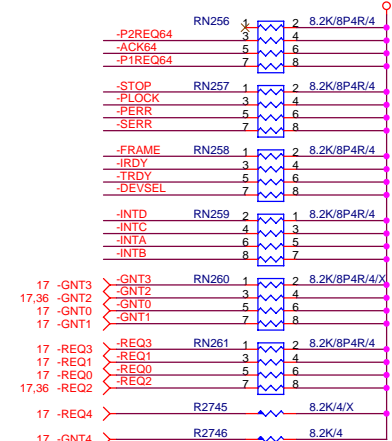
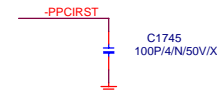
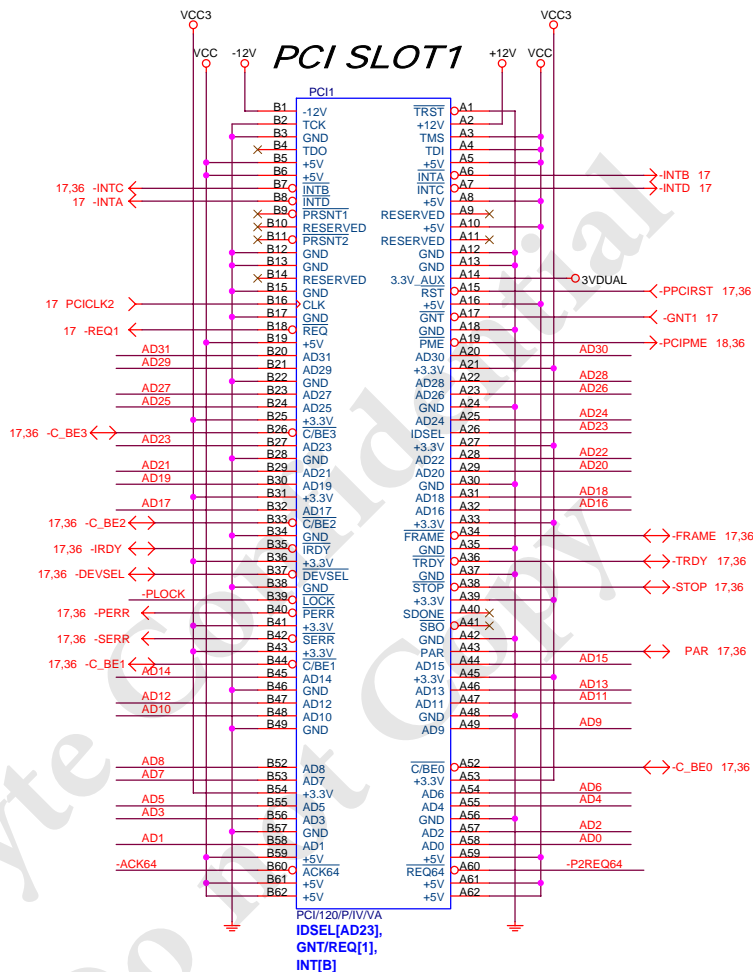


PCI SLOT 1,2

17,36 AD[0..31] ↔ AD[0..31]

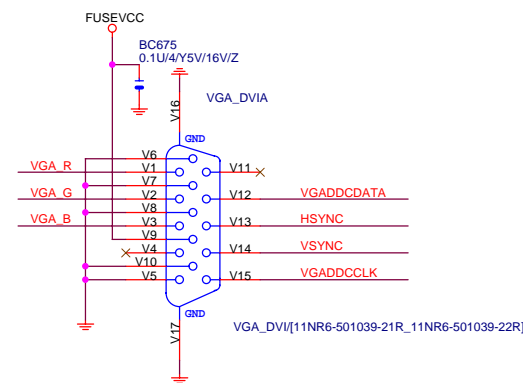
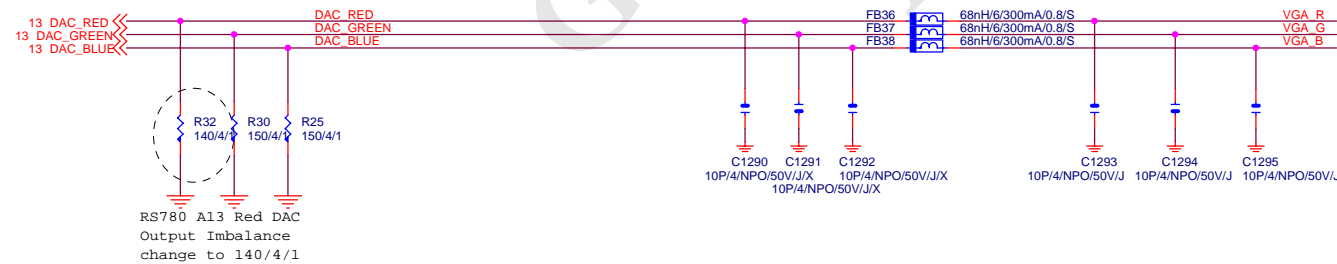
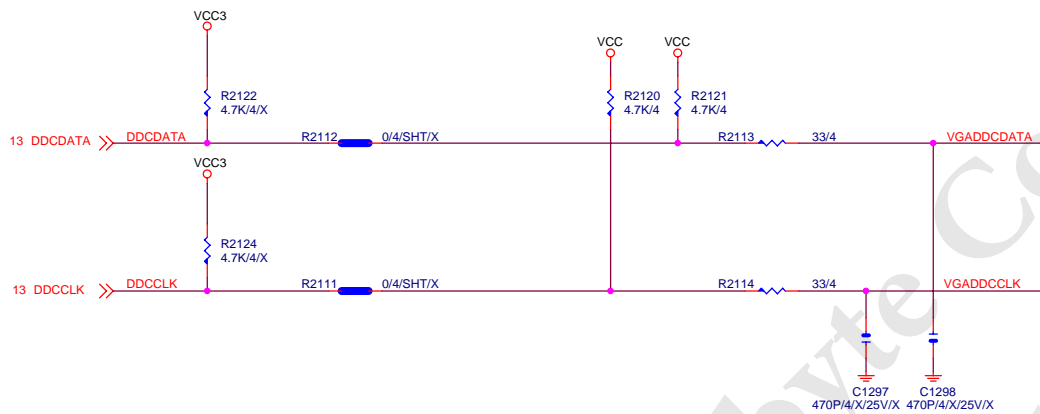
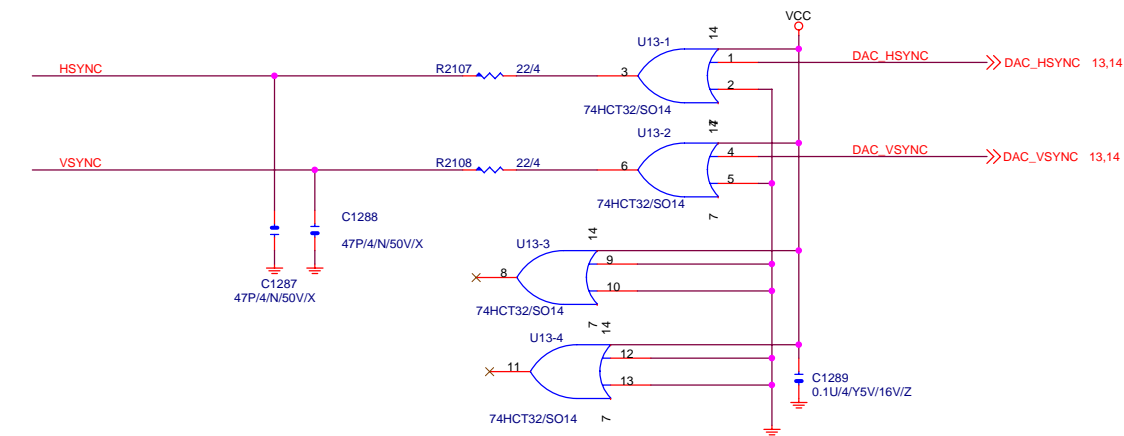


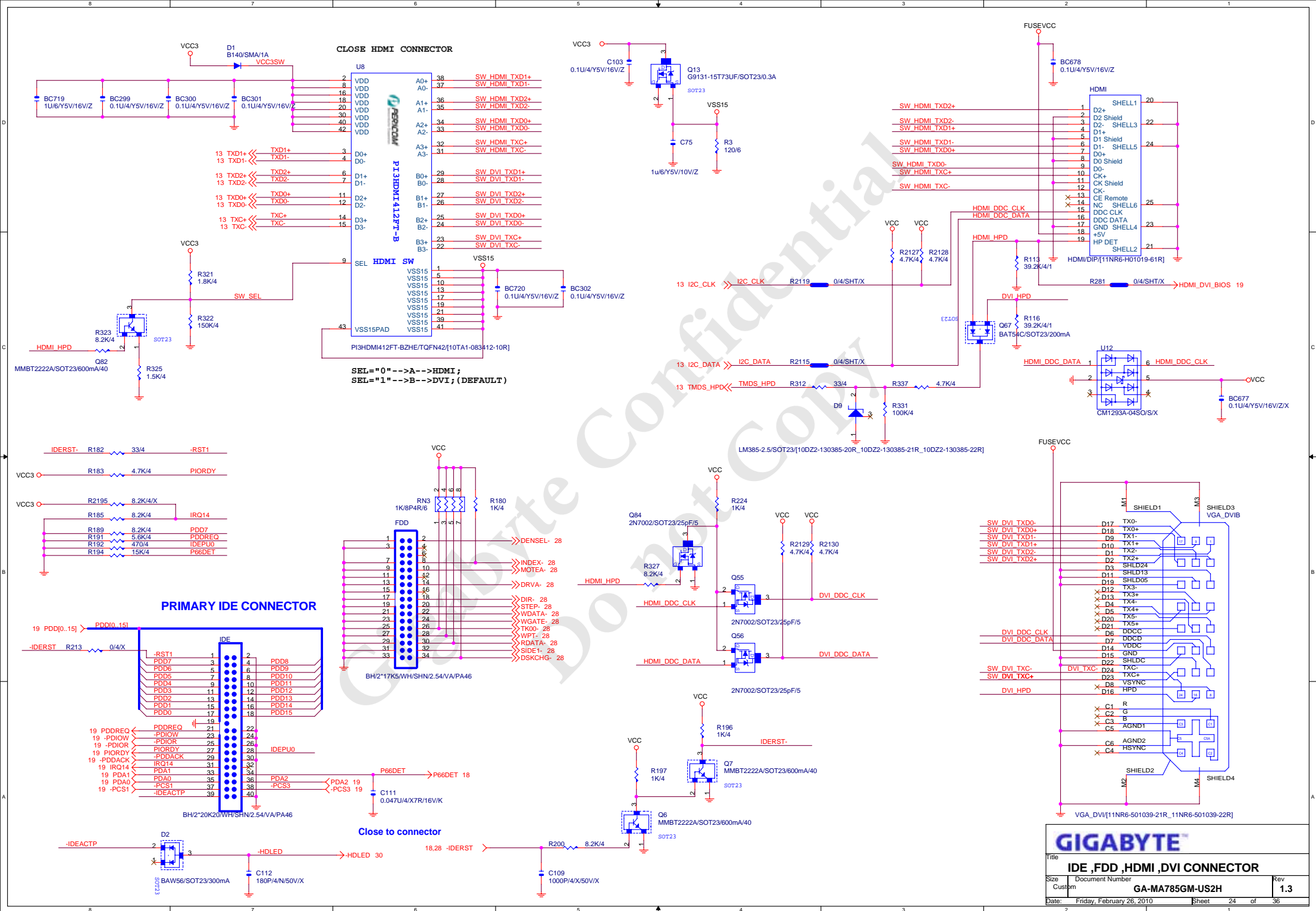
PCI SLOT1

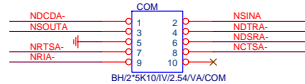
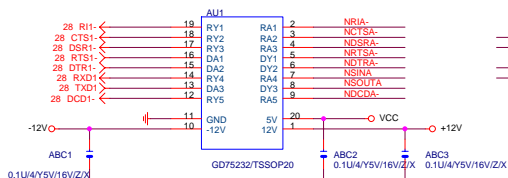


GIGABYTE

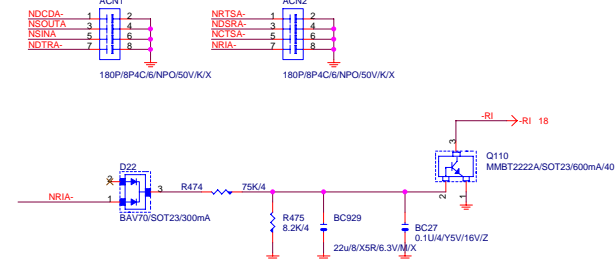
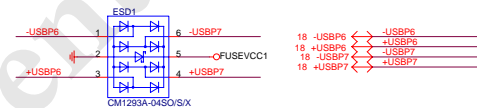
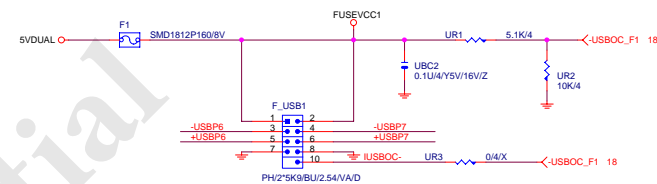
Title PCI SLOT 1,2		
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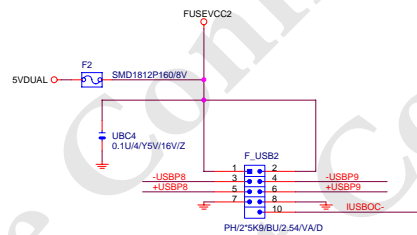




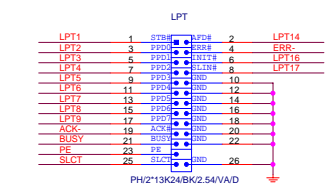
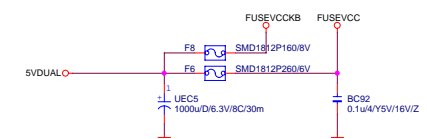
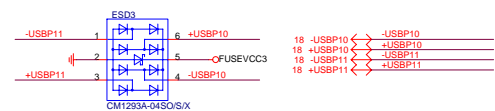
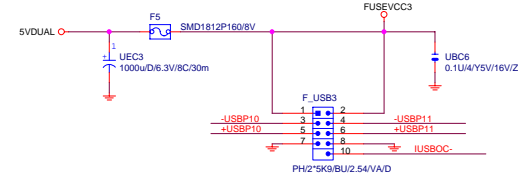
FRONT SIDE USB1



FRONT SIDE USB2



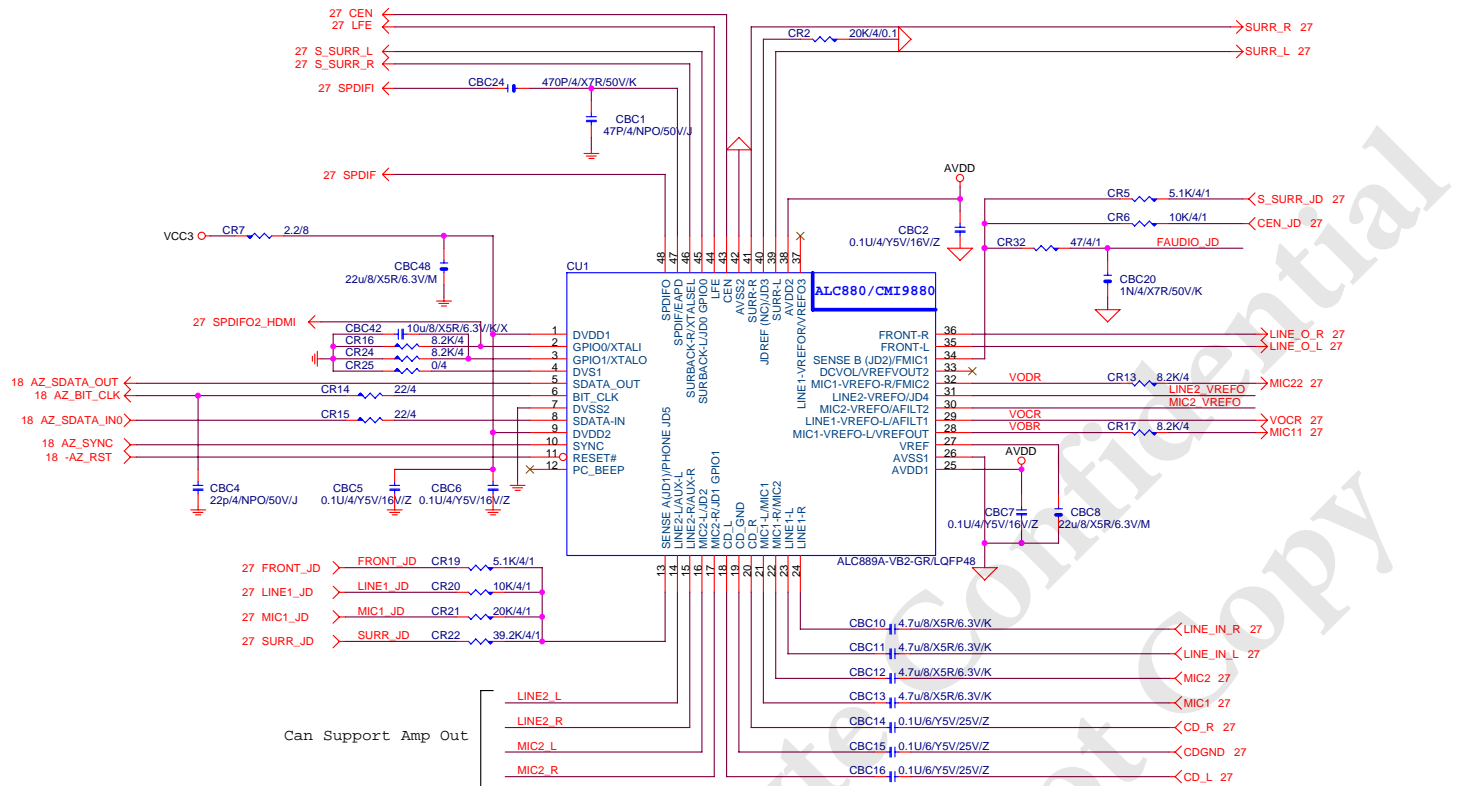
FRONT SIDE USB3



GIGABYTE

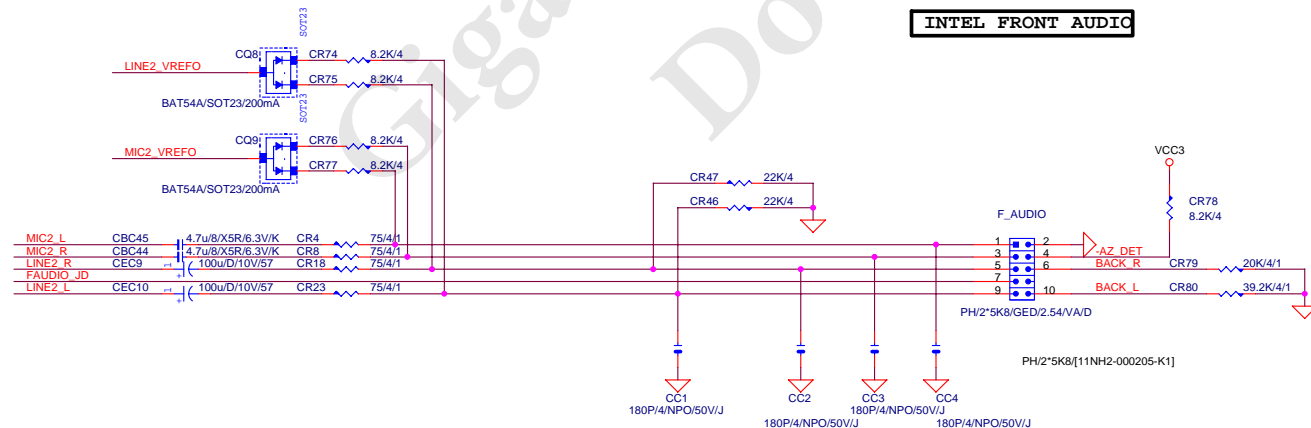
COM/LPT/F_USB

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Can Support Amp Out

INTEL FRONT AUDIO

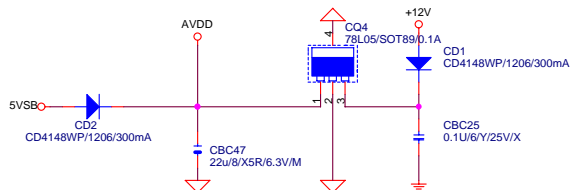
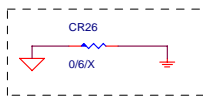


AZALIA CODEC ALC892/ALC889A/ Colay

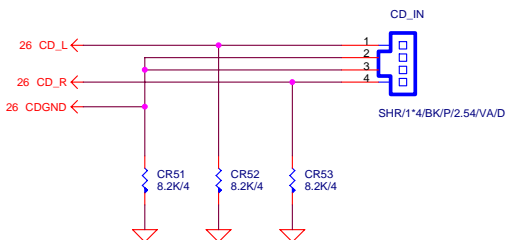
	ALC892		ALC889A
CR16	X		O
CR24	X		O
CR25	X		O
CBC42	10uF/X5R		X
CR2	20K/1%		20K/0.1%
CR9	O		X
CR10	X		O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R		4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR28/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm		75 ohm

GIGABYTE

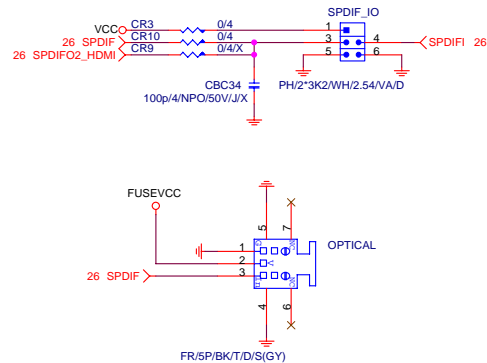
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Size	Document Number	Rev	
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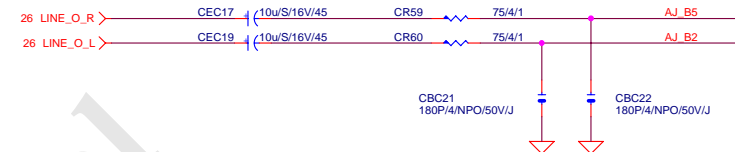
CD IN



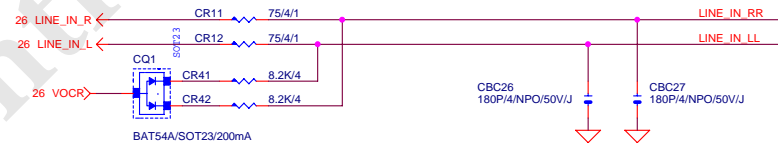
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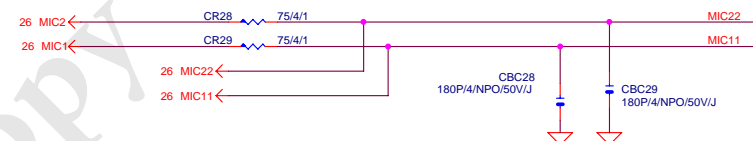
LINE OUT FRONT OUT



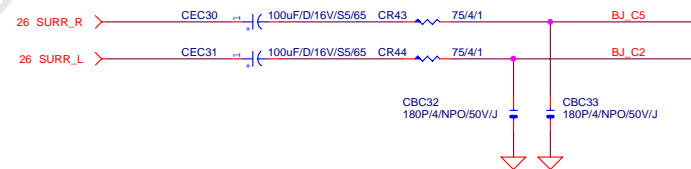
LINE-IN



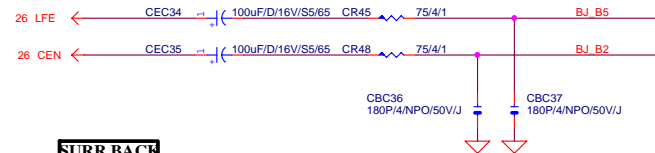
MIC



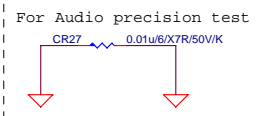
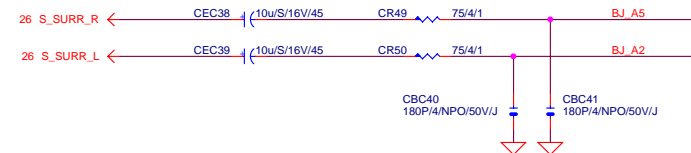
SURROUND



CEN/LFE

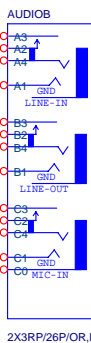
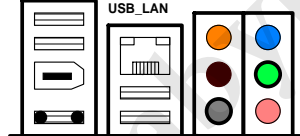


SURR BACK



USB_1394_ESATA

USB_LAN

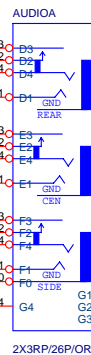


BLUE
LINE-IN

GREEN
LINE-OUT

PINK
MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA



Orange
CEN/LFE

Black
Back side
Speaker

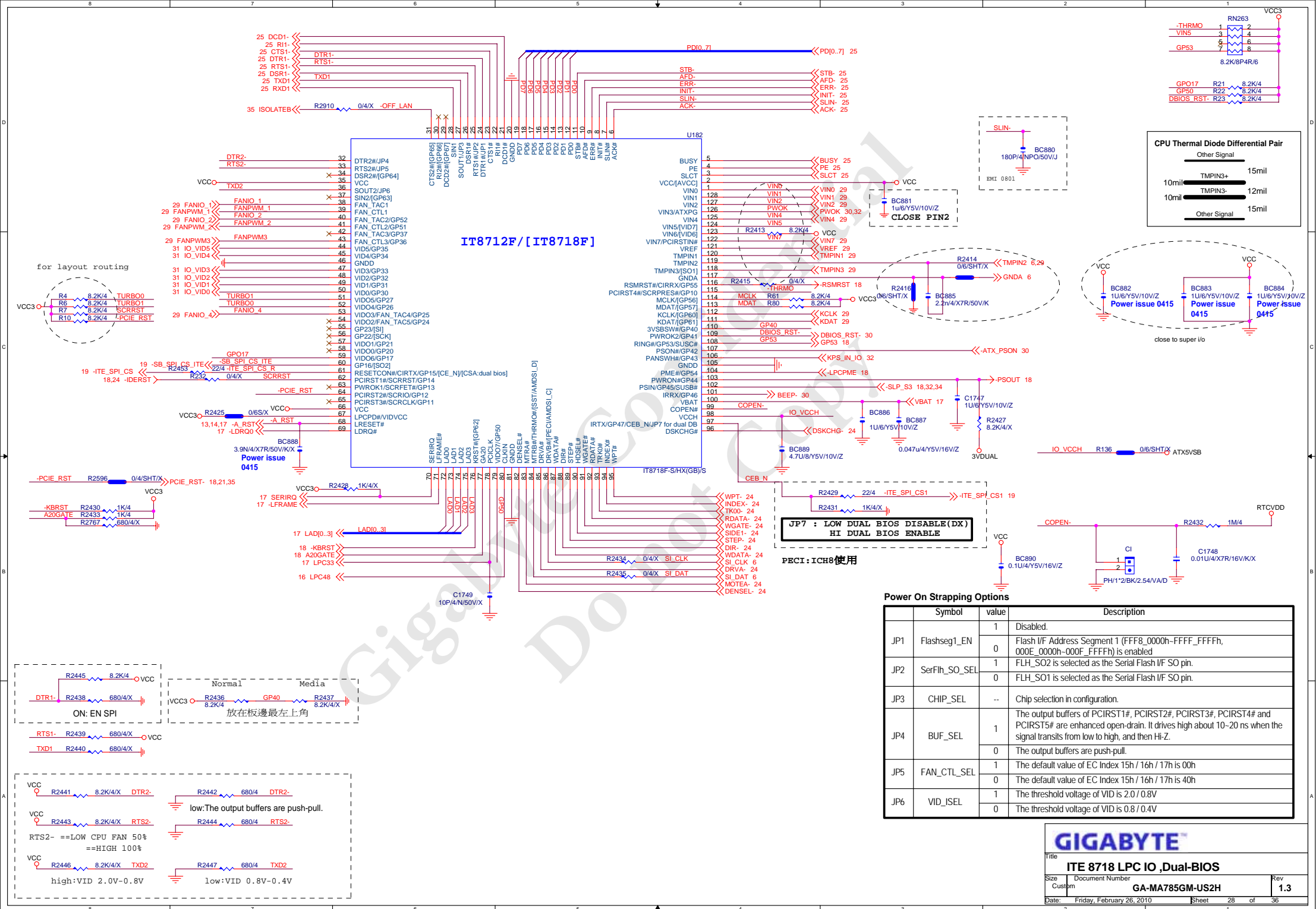
Gray
Left & Right Side
Speaker

ALC880 - SURROUND
CMI9880 - Back SURR
CMI9880 - Side SURR

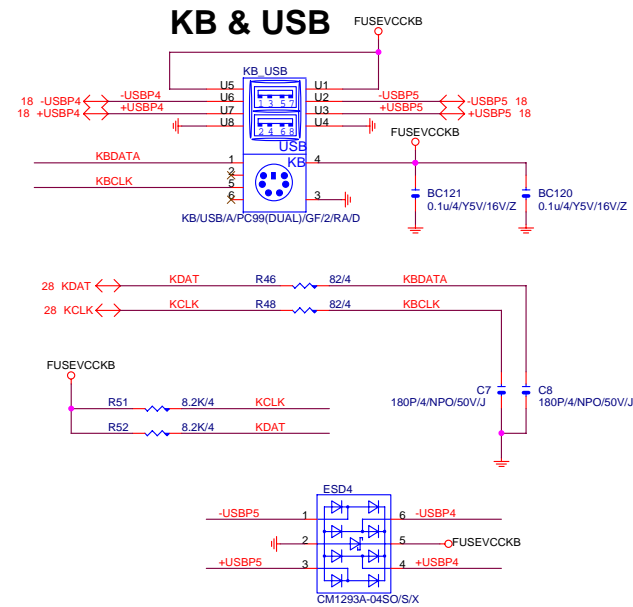
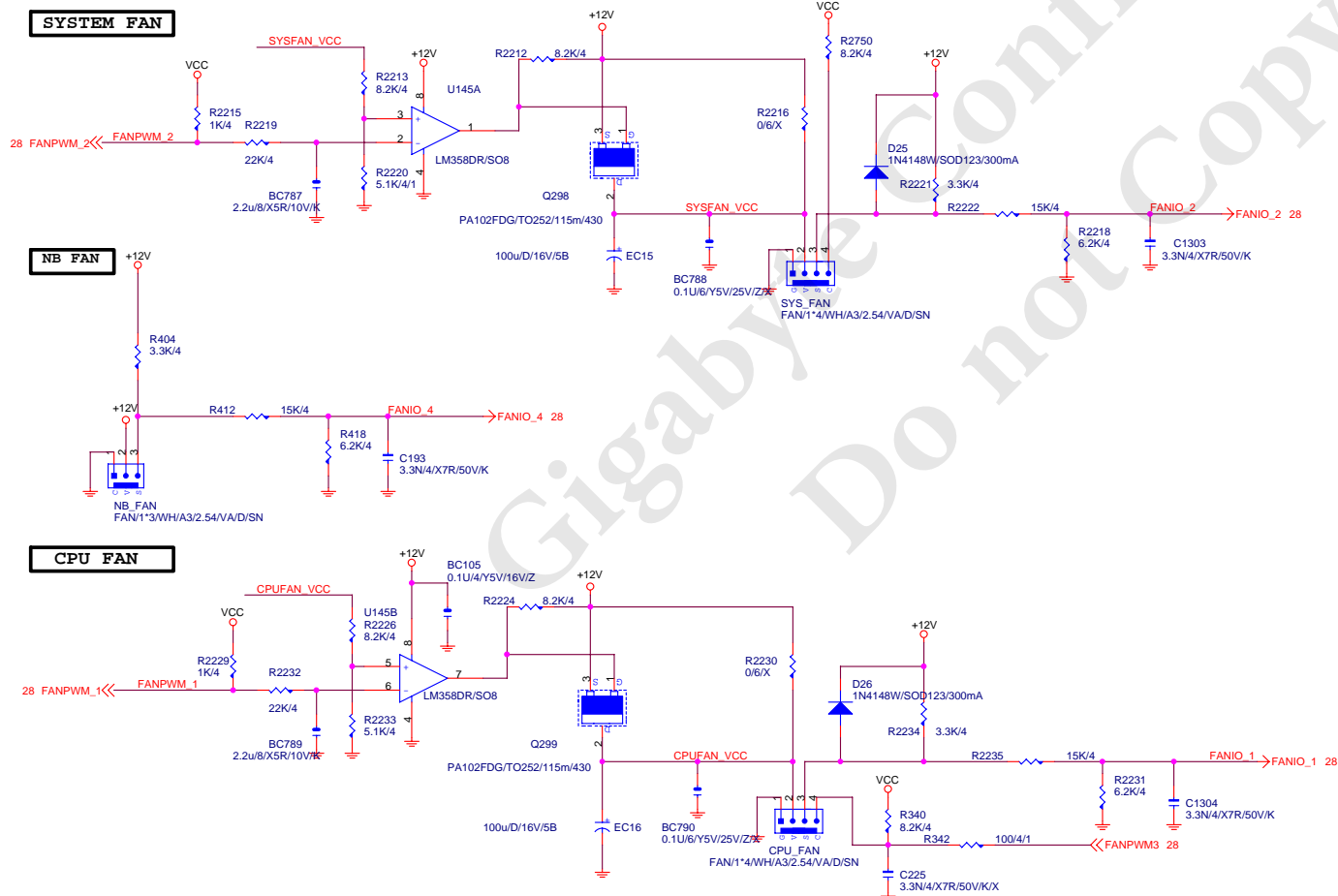
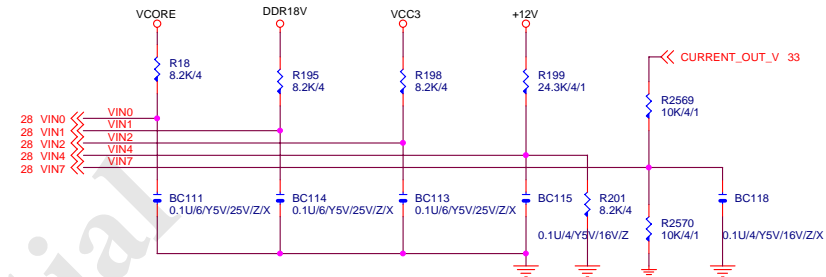
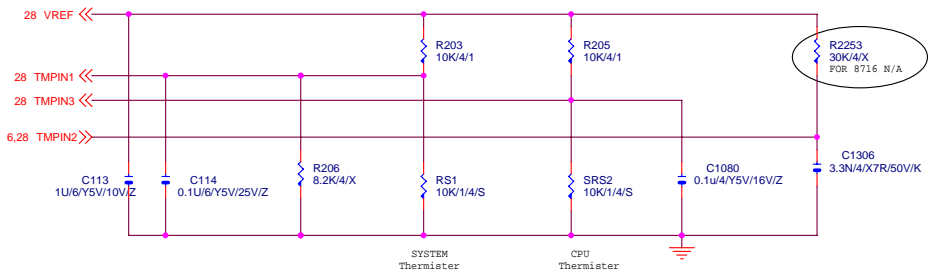
2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

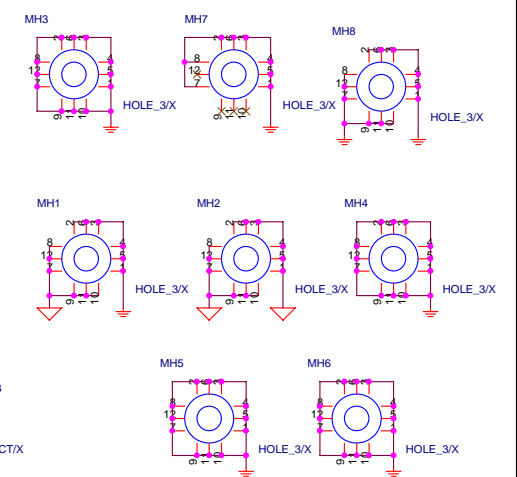
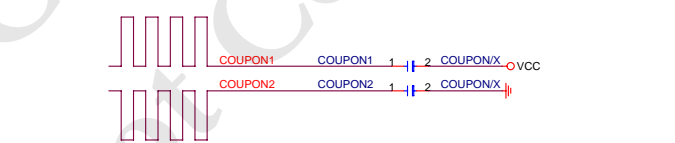
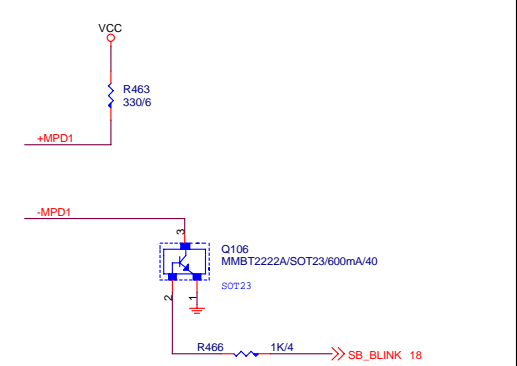
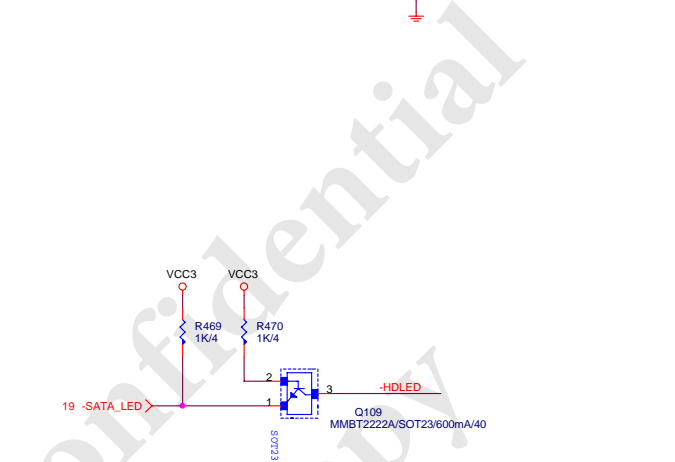
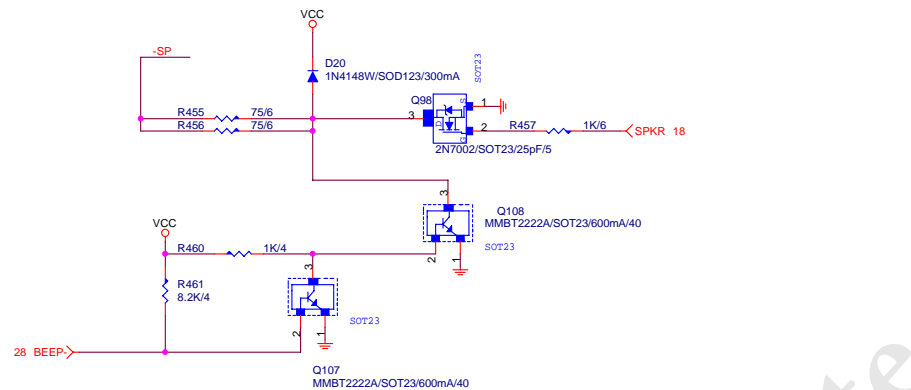
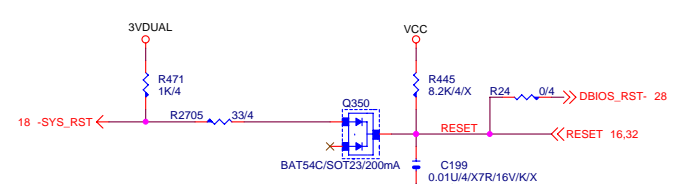
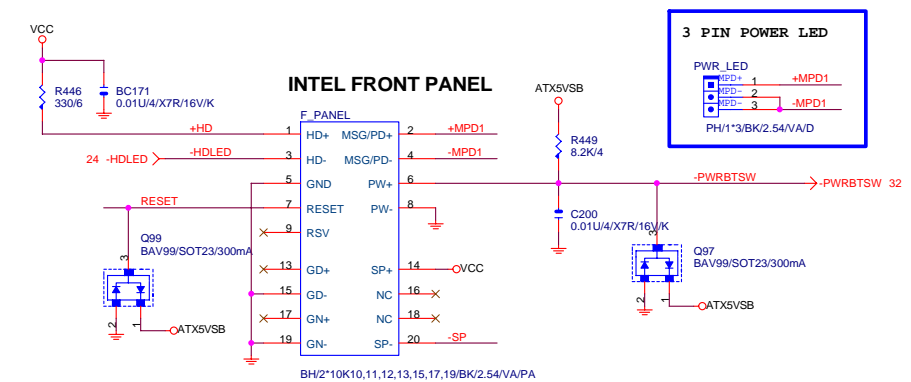
GIGABYTE

Title		
AUDIO JACK		
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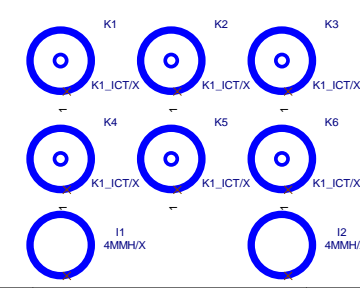


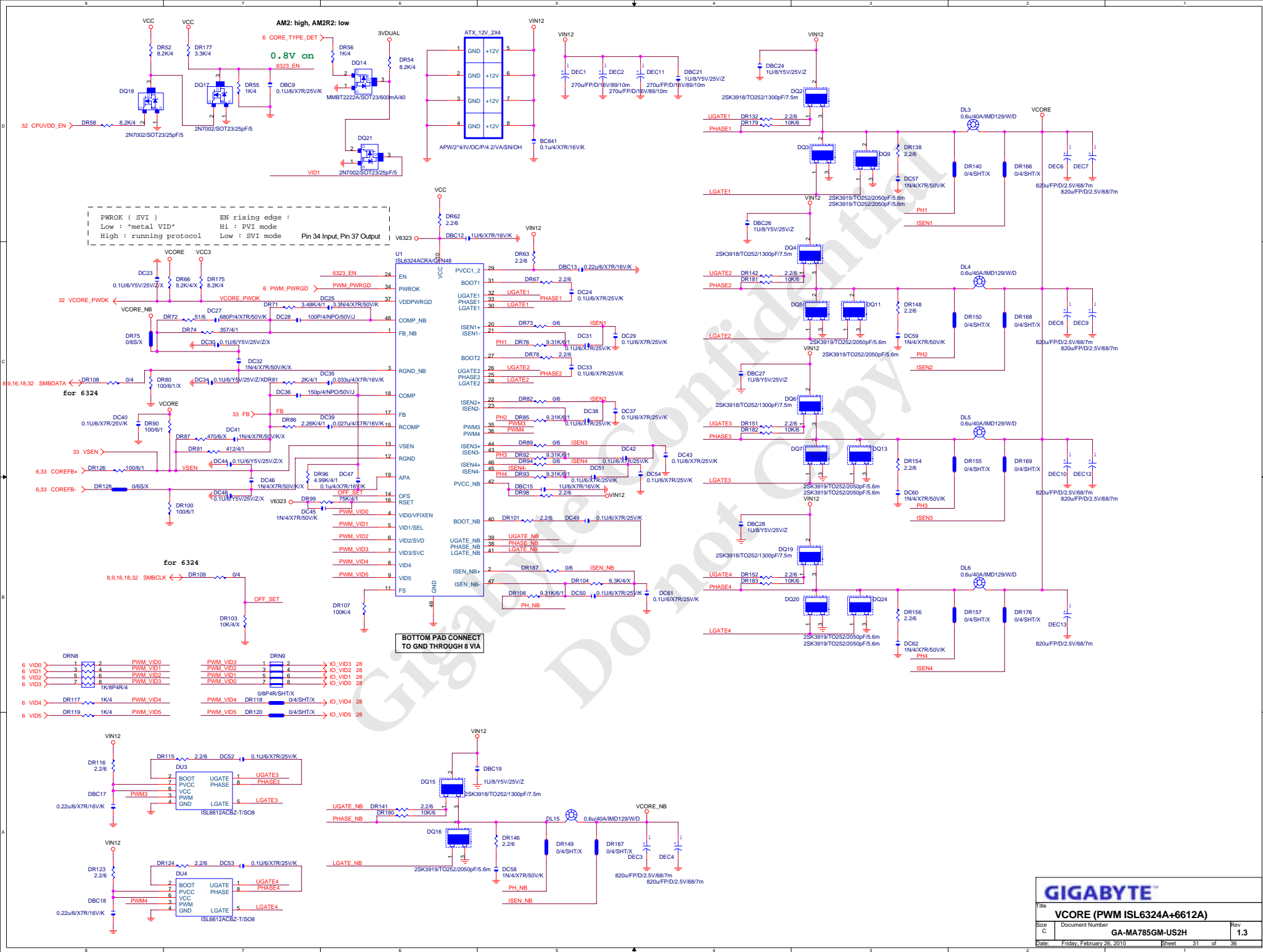
Hardware Monitor circuits

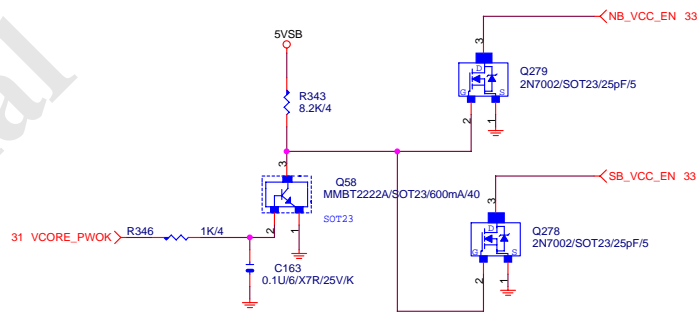
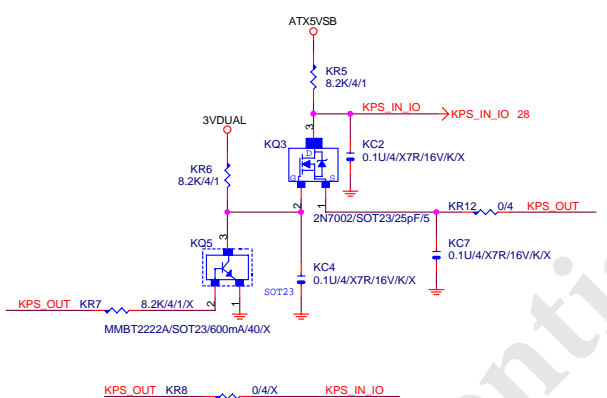
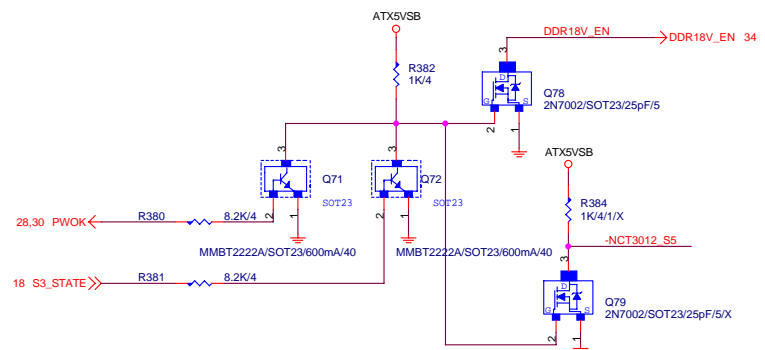




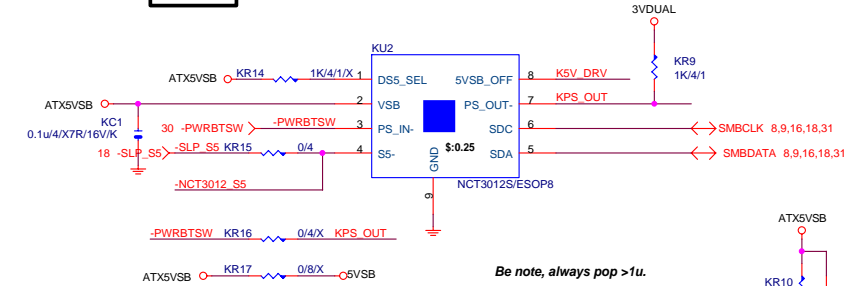
For Seasonic 900W Power supply cant Boot issue





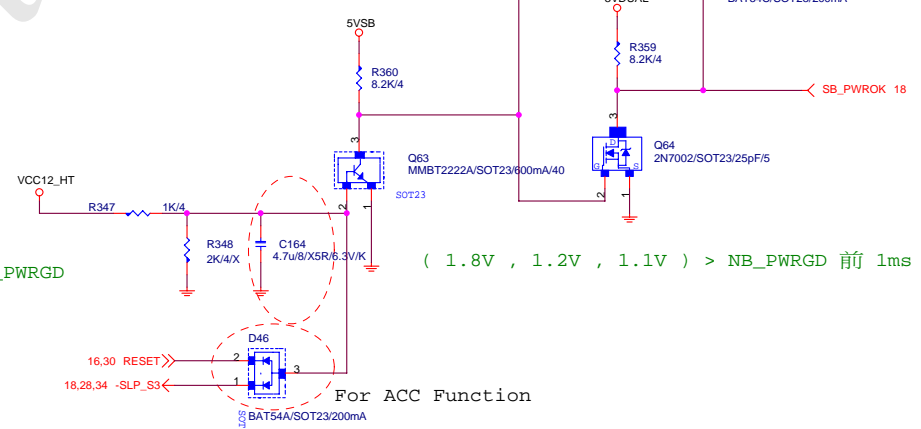
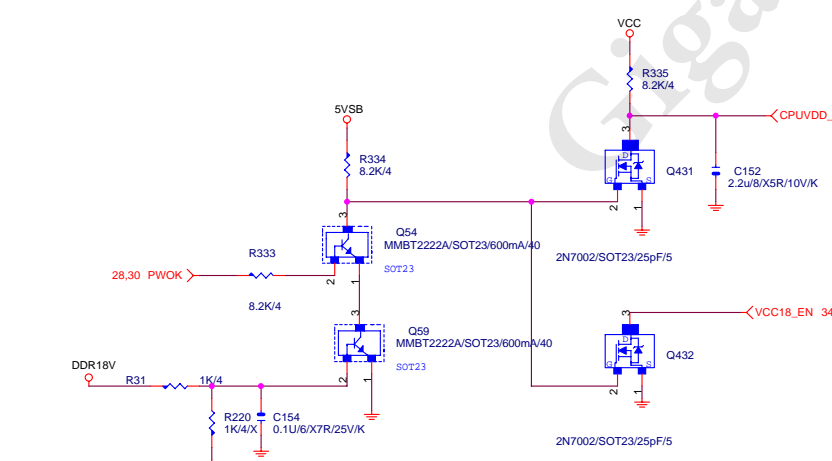


EUP



Function Selection. Strapped by VSB
 Strapped to high :
 DeepS5_Sel = 1:
 System will enter the deep S5 state after 6 sec delays when AC power on.
 Strapped to low : (Default)
 DeepS5_Sel = 0:
 System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.

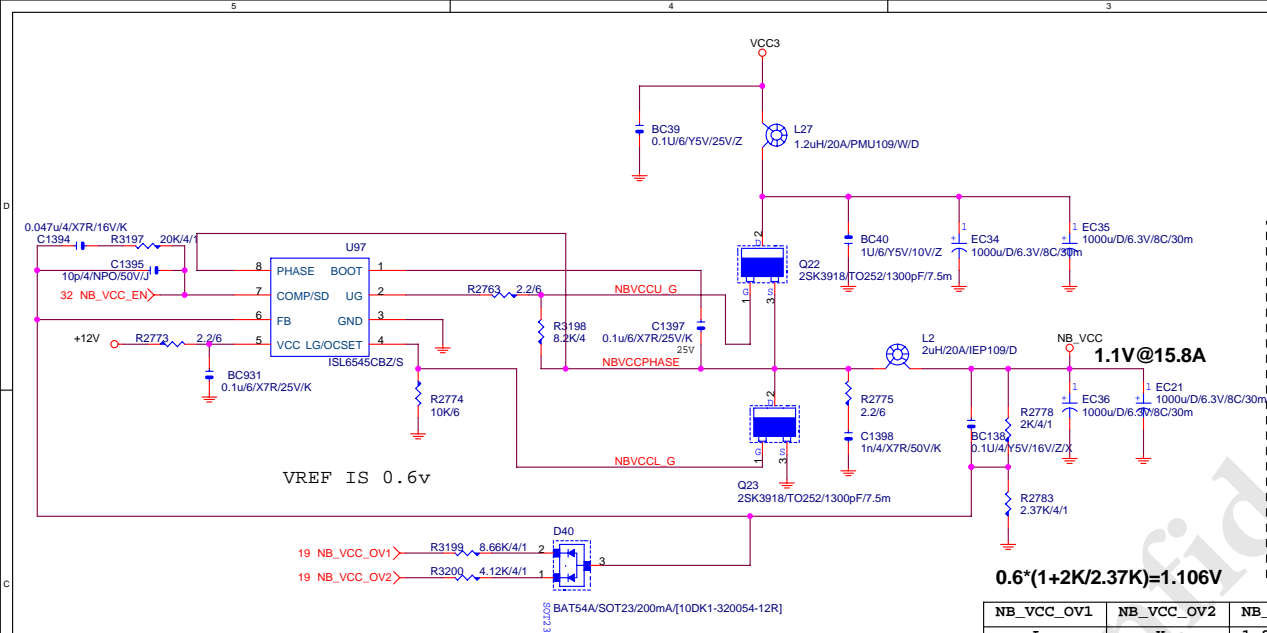
Be note, always pop >1u.



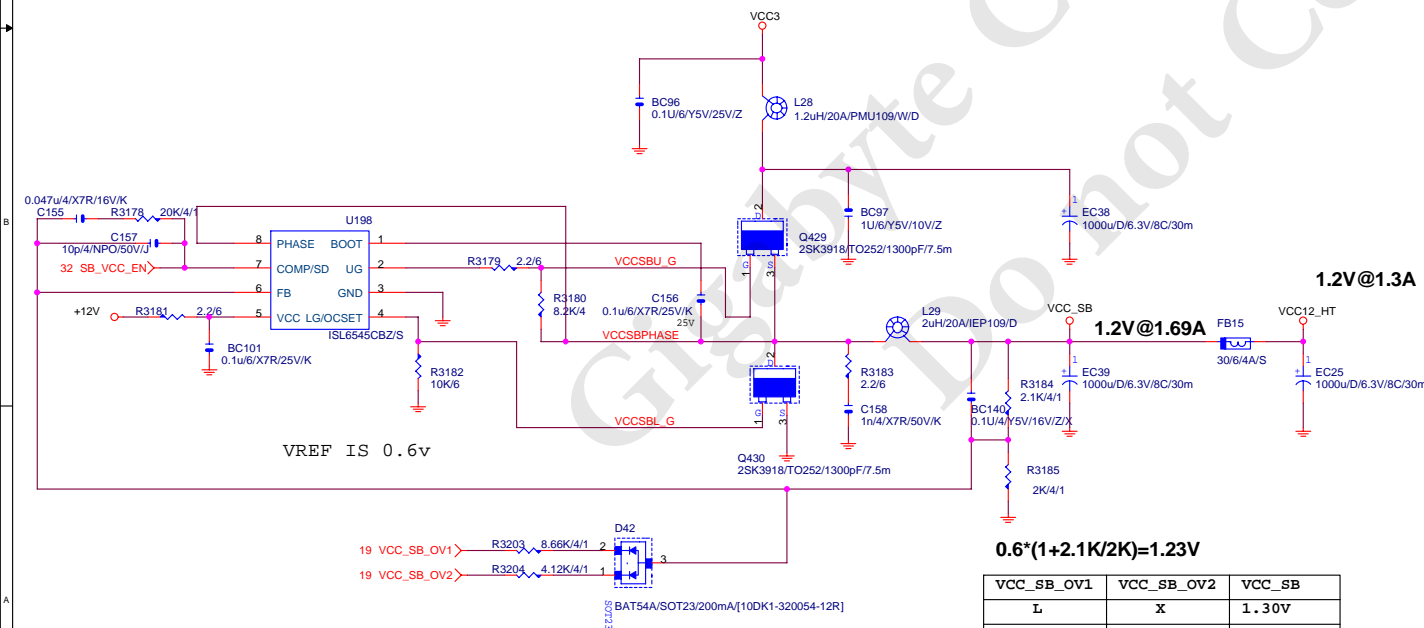
PWOK > NB_PWRGD / SB_PWRGD

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

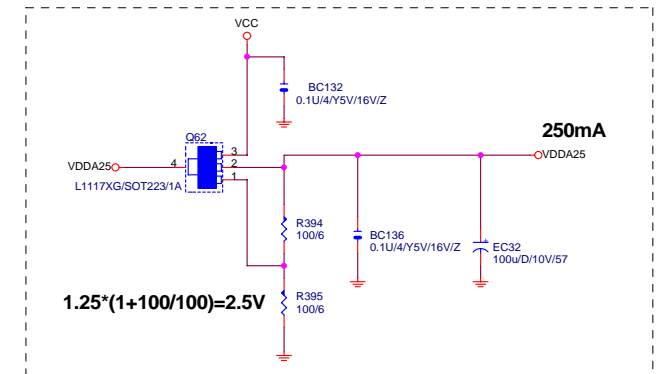
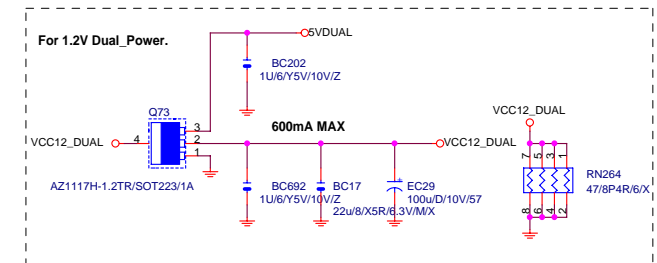
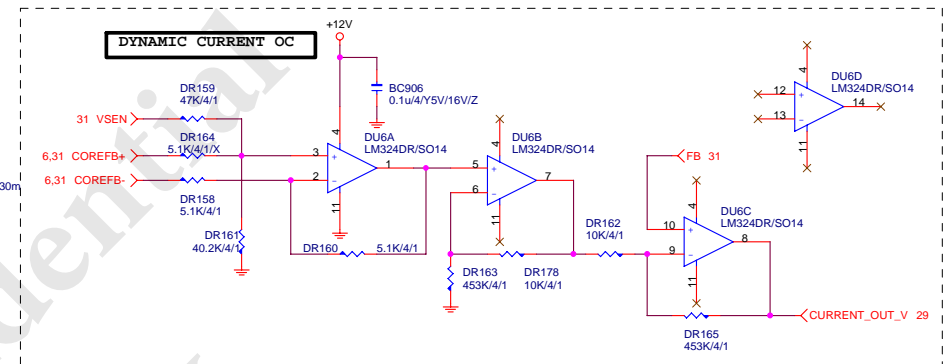
For ACC Function



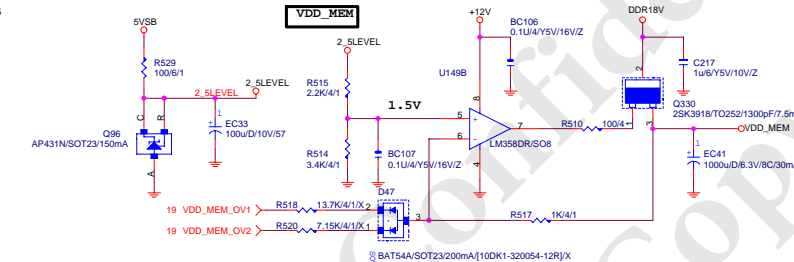
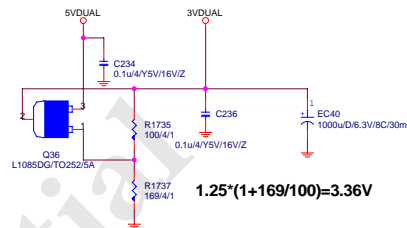
NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V



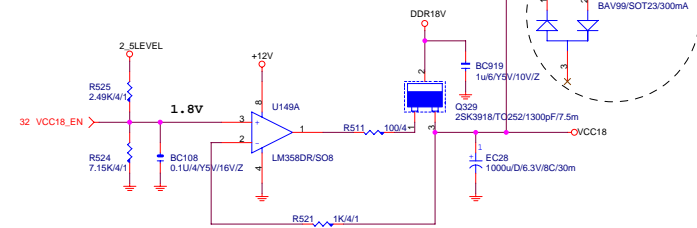
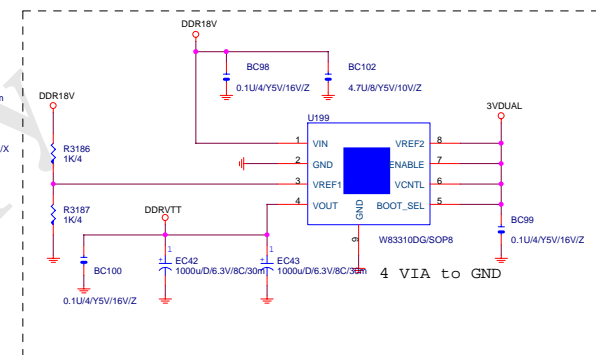
VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V



3VDUAL



VDD_MEM_OV1	VDD_MEM_OV2	VDD_MEM
L	X	1.60V
X	L	1.70V
L	L	1.80V



ATI for vcc3/vcc18 power ramp-up 2.1V

$$0.6 \cdot (1 + 3K/1.43K) = 1.859V$$

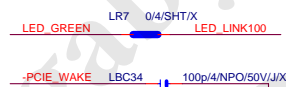
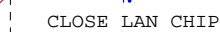
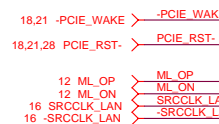
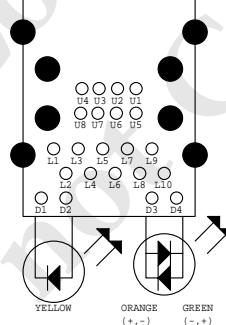
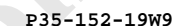
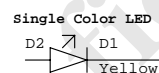
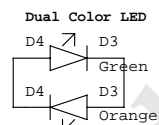
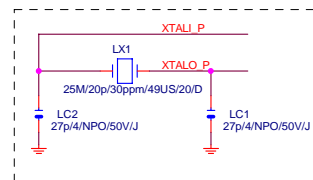
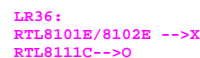
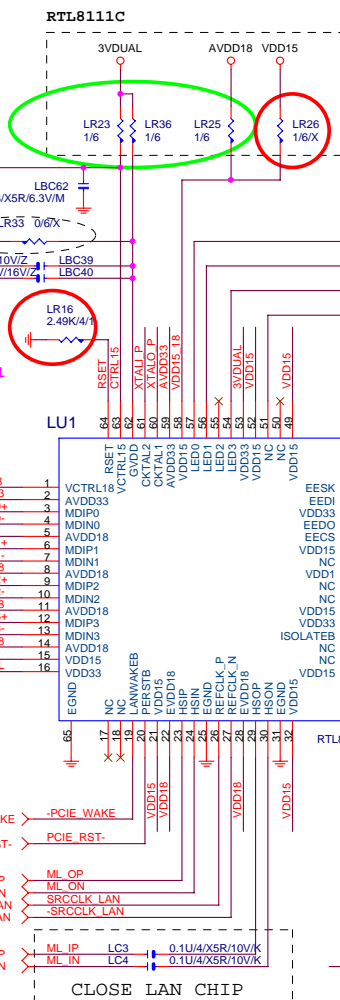
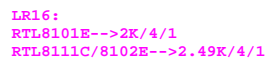
DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V

GIGABYTE™

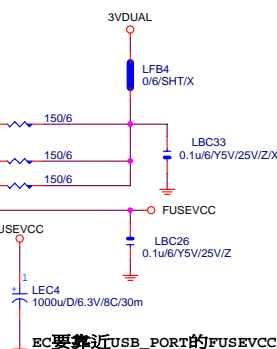
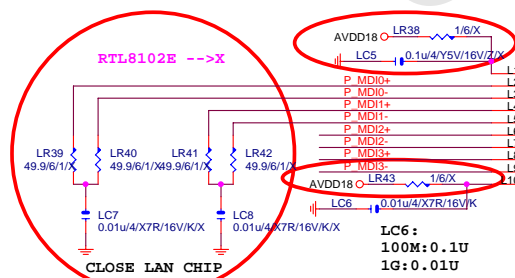
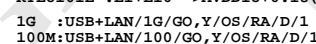
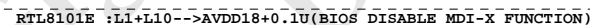
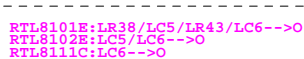
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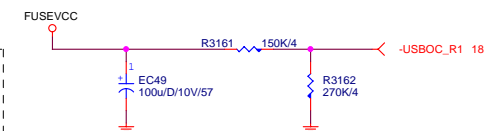
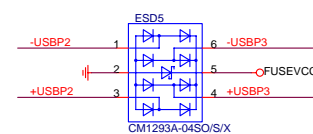
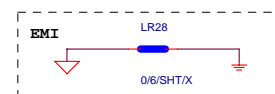
PCIE-1G LAN



USB LAN CONNECTOR



USB LAN



Title	REALTK RTL8111C/8101E
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